A－2－4 A 16-bit microprocessor on SOS -PULCE-

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Advancements of current design and process technique, using N-channel Si-gate MOS/SOS LSI technology, have made it possible to develop a 7000-gate general purpose computing element on a chip, a high speed 16-bit parallel microprocessor called PULCE, which stands for Pips* UniversaL Computing Element. This paper describes the newly developed Coplanar-II process for SOS LSI and the chip organization, the function and the performance of PULCE.

A conventional air isolation method tends to have several disadvantages such as low gate breakdown voltage and anomalous drain leakage currents and, furthermore, metal interconnection breakage due to steps of the MOS/SOS LSI surface. In order to improve them, a coplanar process was applied to SOS LSI. The essential points of the Coplanar-II process are as follows. The silicon film prepared is 0.7 um thick and (100) high resistive P-type. The silicon film is first covered with thermal oxide and, then with a Si_3N_4 film. The Si_3N_4 and thermal oxide in the field region are selectively etched, then the silicon film is etched to a halfway of the thickness. The remaining silicon film in the field region is completely oxidized with Si_3N_4 as a mask. Then the Si_3N_4 film is removed and 800A thick gate oxide is formed. After the process step, a conventional N-channel Si-gate process is used. It should be noted that the step difference between the top surface of the silicon island and that of the field oxide is minimized to prevent breakage in interconnection. To minimize drain leakage currents in N-channel MOS/SOS transistor, the field oxidation time and temperature had to be reduced by etching the upper part of silicon film in the field region before field oxidation.

The Coplanar-II process was successfully used tc fabricate a N-channel Si-gate depletion load MOS/SOS LSI CPU, PULCE, which utilizes a 4um channel length design rule. The chip contains approximately 7000 gates or 20000 transistors in an area of 8.25mm x 6.66mm and is packaged in a 80-pin flat package. It operates on a single +5V power supply and a single clock input. The photomicrograph of the chip appears in Fig.1. The architecture of the PULCE is designed to maximize a flexibility to general purpose computing system applications, which provides powerful arithmetic and logical functions and a detailed micro-programing capability. Figure 2 shows the functional block diagram of PULCE. The circuits are designed with a parallel 16-bit three-bus system. The shifter operates multi-

* Pips; Pattern information processing system

bit shift within 15 bits in one machine cycle. The ALU has one digit decimal adder /subtracter. The general registers can be connected up to 4 words length (64 bits) and act as one-bit shift registers in one machine cycle. The features of the register file 0 include operation of an internal stack. Seven words of the register file 1 can be act as mask data to three busses. In order to be flexible, external and procedural control functions such as branch, I/O and memory access instruction etc. are left to external control circuits. A 32-bit micro-code is given by external micro-program memories. PULCE has two 16-bit data-ports which can be used as interface registers in the system.

The drain leakage current in the N-channel MOS/SOS transistor fabricated by the Coplanar-II process is typically 7×10^{-11}A/8um, which assures the dynamic operation of transfer gates in the registers. The gate oxide dielectric breakdown field strength is typically 8.7MV/cm, which is more than two times of that for a conventional air isolation process. Typical machine cycle time is 250nsec. and the power dissipation is 1.5W. The machine cycle time in a micro-instruction execution is shared as follows. Both micro-code decoding time and access time of registers take 24% of the machine cycle time. ALU operation requires only 22% of it. Transfer of the ALU output consumes 30% of the cycle time. The values verify that, in a LSI CPU, ALU operation time is not dominant in the cycle time but the propagation delay of control signals and data transfer times occupy the most of the cycle time.

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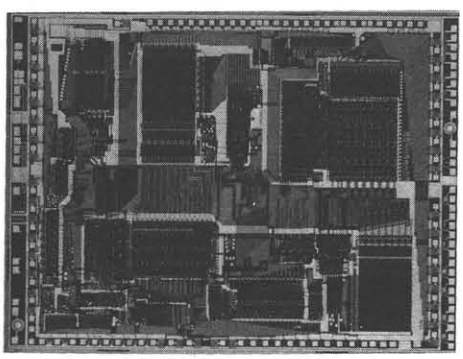

Fig.1 Photomicrograph of PULCE

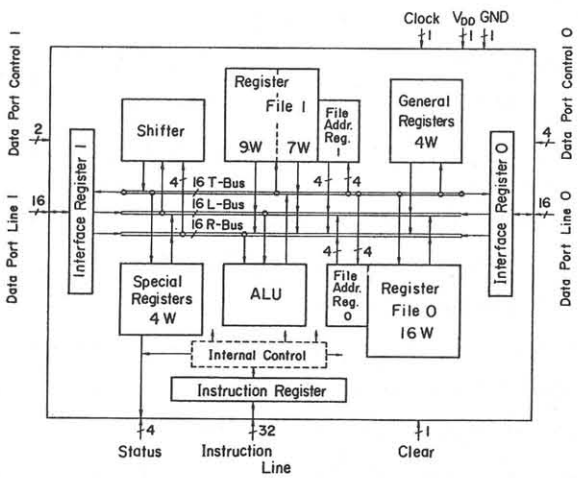

Fig.2 Block diagram of PULCE