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High Packing Density, High Speed CMOS(Hi-CMOS) Device Technology

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High performance MOS technology achieved by microfabrication techniques has been mainly applied to high performance n channel MOS(H-NMOS) devices. However, H-NMOS devices have poor device margins due to short channel effects and have the power dissipation limitations of large scale integrations(LSIs). Complementary MOS(CMOS) devices overcome these drawbacks, but conventional CMOS devices have disadvantages of low packing density and low operatig speed. If these poor characteristics can be improved through new technology, CMOSs will become ideal devices for achieving high performance MOS LSIs.

In this paper, a new high performance CMOS(Hi-CMOS)technology is described which provides high packing density, high speed CMOS LSIs. Hi-CMOS is basically a short channel device whose gate length is about 3 μm. To improve device characteristics, the device structure dimensions(gate oxide thickness, junction depth) are reduced in size as H-NMOS devices have been.

A new device structure is realized in Hi-CMOS as shown in Fig.1. Both the n channel and p channel transistors are fabricated in the wells formed by ion implanted impurity diffusion in high resistive substrate. This structure permits independant control of the surface impurity concentrations of both wells. The impurity concentration of both wells is designed optimally to reduce the junction capacitance and substrate constant. Therefore, the threshold voltages of both channel transistors are well controlled by precise ion implantation channel doping, whereas conventional CMOS threshold voltages are basically controlled by the substrate(or well) high impurity concentration. The junction depth of the p-well is decreased to reduce the distance from the n channel to p channel transistors, which contributes to the high packing density of the Hi-CMOS.

The I-V characteristics of Hi-CMOS n channel and p channel transistors are shown in Fig.2. The absence of a lateral bipolar effect in p channel transistors leads to high breakdown voltages. Large channel conductance of the Hi-CMOS is obtained by the channel doping method which reduces the impurity concentration of wells. Other Hi-CMOS features are depicted in Figs.3 and 4. The substrate bias constant and the junction capacitance are also decreased to one half in comparison with conventional CMOS method structures. The Hi-CMOS threshold voltage dependence on gate length is shown in Fig.5. The short channel effect

on threshold voltage is reduced by the Hi-CMOS structure. Moreover, in view of threshold voltage controllability, the non-use of back bias voltage in Hi-CMOS devices is superior when compared with back biased H-NMOS devices.

The inverter chain was fabricated by the Hi-CMOS technology and showed 0.55 nsec. delay time per one stage which is the same as for H-NMOS. The Hi-CMOS inverter power dissipation is one or two order of magnitude less than for H-NMOS as shown in Fig.6. Hi-CMOS technology can be most suitably applied to high speed, low power dissipation memories. Fabricated 4K-bit Hi-CMOS static RAMs had a 40 nsec. typical access time which is the highest speed achieved by 4K-bit MOS RAMs. The power delay product of Hi-CMOS 4K-bit memories is one order of magnitude smaller than with an H-NMOS memory.

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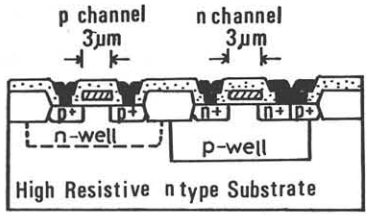

Fig.1 Hi-CMOS Device Structure.

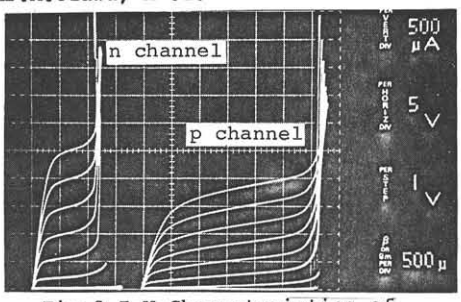

Fig.2 I-V Characteristics of Hi-CMOS Devices.

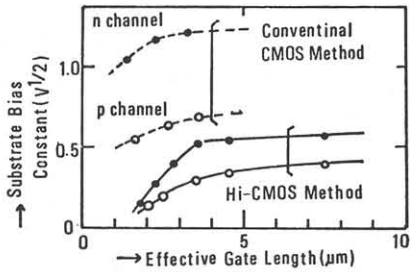

Fig.3 Substrate Bias Constant of Hi-CMOS.

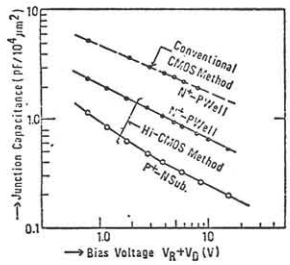

Fig.4 Junction Capacitance of Hi-CMOS.

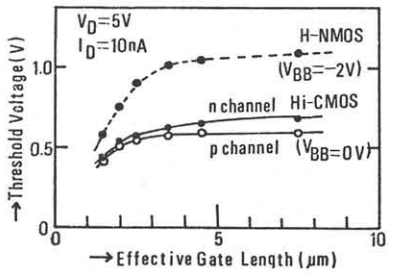

Fig.5 Threshold Voltage Dependence on Gate Length.

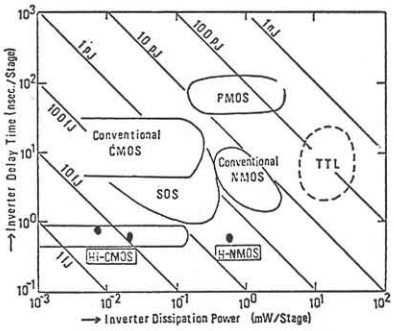

Fig.6 Inverter Delay Time and Power Dissipation of Hi-CMOS.