

A-3-2

High Speed 1 K Bit Static RAM using DSA MOST's

K. Kobayashi, M. Saitoh, Y. Murao and K. Takahashi*

IC Division, Central Research Labs.,^{*} Nippon Electric Co., Ltd.
1753, Shimonumabe, Nakahara-ku, Kawasaki, 211, Japan

This paper describes a newly developed high speed (10 ns) 1 K bit static RAM with 5 V single supply voltage, using an improved DSA short channel ED MOS technology and an improved circuit design.

Concerning the dimensional reduction of structure, following considerations have been made. First, fine mask patterns were realized by using posi-type photoresist; the minimum line width of 3.5 μm for aluminum and the minimum area of 2 μm x 2 μm for contact holes. Second, an improved poly-silicon interconnection technology¹⁾ was applied for realizing the minimum line width of 3 μm with low sheet resistance of $\sim 10\Omega/\square$, without the sacrifice of shallow junction depth for source and drain regions. In addition, thin gate oxide thickness of 300 \AA , a shallow junction depth of 0.5 μm , and short channel lengths of 2 μm for DSA MOST's and 4 μm for load MOST's were used.

Figure 1 shows the cross section of a DSA-ED-MOS inverter. 100 \sim 150 Ω -cm p-type silicon was used as a substrate. The threshold voltage of DSA MOST's was well controlled by the use of refined ion-implantation technique. Load MOST's with the threshold voltages of -5 V and 0 V were used, the one with phosphorous implantation and the other without it.

Figure 2 shows a typical I_D - V_D characteristics of the DSA MOST for $V_G = 0 \sim 6\text{V}$. Channel modulation is hardly observed, and a gain constant of 1.6 mS/V for $W = 100 \mu\text{m}$ is obtained in the triode region for $V_G = 5\text{V}$, $V_D = 0.5\text{V}$. This value is larger by about 20% than that of a conventional MOST with the same dimension.

The present RAM is designed to be TTL compatible, fully static and to operate on a single 5V power supply without an internal bias generator. For high speed required parts, such as address and data buffer push-pull circuits, lower threshold voltage (-5 V) load MOST's are used. In the push-pull decoder buffers and memory cells, on the other hand, higher threshold voltage ($\sim 0\text{V}$) load MOST's are applied, to reduce power dissipation. A conventional six transistor memory cell is used, and the transfer gate consists of a DSA MOST whose drain electrode is connected to the digit line. A main sense amplifier is improved to consist of a pair of refined amplifiers with common load MOST's. Therefore, a pair of read bus lines can be divided into two pairs to decrease the stray capacitance of a read bus line by half.

Figure 3 shows a microphotograph of the DSA static RAM chip. The cell dimension is 30 μm x 51 μm and the chip size is 1.97 mm x 3.05 mm. Figure 4 shows the address input and data output signal waveforms for 32.5 pF output load capacitance. The address access time is 10 ns, which increases by 1 ns for an additional 20 pF output load capacitance. Figure 5 shows the dependence of address access time T_{acc} on supply voltage V_{DD} . The T_{acc} has a minimum value near $V_{\text{DD}} = 5$ volts

and is almost constant for $V_{DD} = 4.5 \sim 6.0$ volts. Figure 6 shows the dependence of total current I_{DD} on V_{DD} . The power dissipation is 480 mW for $V_{DD} = 5$ volts. As shown in the figure, memory cell data are retainable for $V_{DD} \geq 1.2$ volts, and a read-write operation is possible for $V_{DD} \geq 4.0$ volts.

In summary, a high speed 1 K bit static RAM with 10 ns address access time has been developed using DSA ED MOST's, a fine pattern technology and an improved circuit design.

The authors are grateful to H. Yamanaka and T. Taguchi for their advice in the device processing. They also wish to thank Drs. T. Okada and N. Kawamura for their continuous encouragement during this work.

A part of this work was accomplished under the contract with the Agency of Industrial Science and Technology for Research and Development of a Pattern Information Processing Systems, Japan.

Reference 1) T. WADA et al., ECS Fall Meeting, vol. 77-2 (1977), pp. 869-870

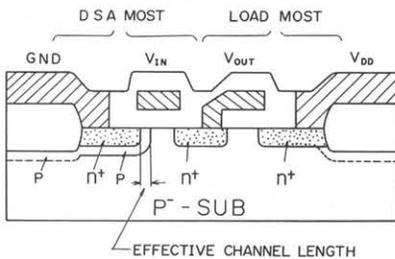


Fig. 1 Cross section of a DSA-ED-MOS inverter

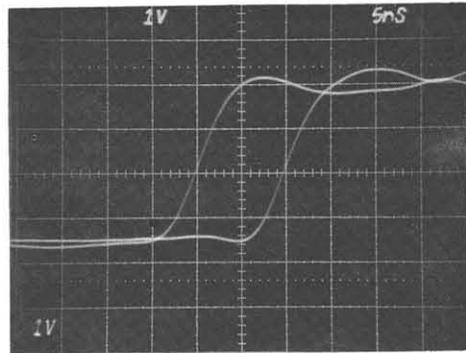


Fig. 4 Address input and data output signal waveforms

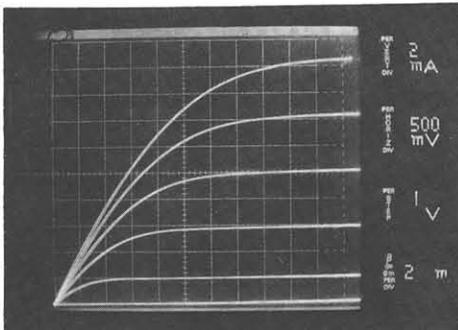


Fig. 2 $I_D - V_D$ characteristics of the DSA MOST

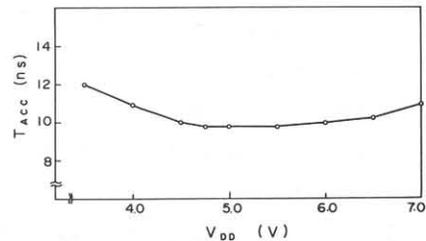


Fig. 5 Dependence of address access time (T_{acc}) on supply voltage (V_{DD})

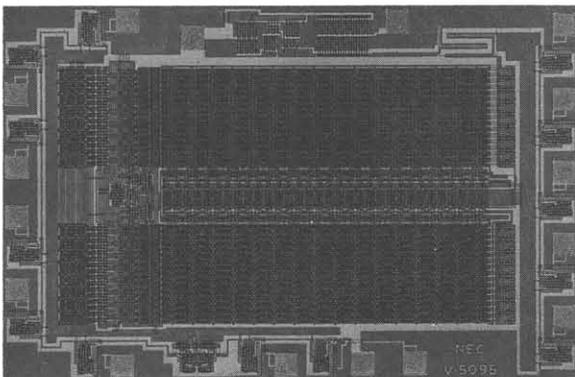


Fig. 3 Microphotograph of the DSA static RAM chip

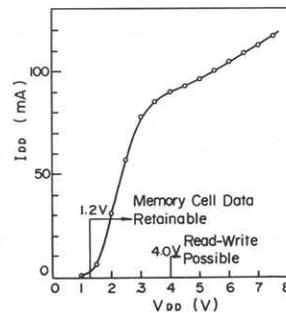


Fig. 6 Dependence of total current (I_{DD}) on supply voltage (V_{DD})