A 64K Dynamic MOS-RAM Using Short-Channel, Channel-Dope Technology

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A 64K dynamic MOS-RAM organized as 16 kwords X 4 bits has been realized by short-channel, channel-dope technology. Also, the improved low power sense amplifiers and a multiplexed address system have been developed. The access time and power dissipation are 110 ns and 150 mW, respectively, at the cycle time of 400 ns.

The innovative single-level Si-gate MOS technologies employed for the present 64K dynamic RAM are summarized as follows: 1. Lightly doped Si substrate, $n_0=10^{15}$ cm$^{-3}$; 2. Thin SiO$_2$ gate film thickness, 400 Å; 3. Phosphorus diffused shallow junction depth, 0.5 μm; 4. Short effective channel length having channel dope region, 2 μm; 5. Low poly-Si sheet resistivity, 13 ohm/µm.

Typical gate threshold voltage of an MOS transistor is 0.85 V for 1 V drain voltage. The effect of channel dope will be summarized later.

A photomicrograph of the 64K RAM and its mask layout are shown in Figs. 1A and 1B, respectively. The chip area is 4.72 mm X 7.05 mm which is assembled in a standard 22 pin DIP package. The memory cell size is 15 μm X 18 μm in which poly-Si word and aluminum bit lines cross each other. The RAM chip has four pads for data-in and four others for data-out, and fourteen addresses are multiplexed on seven address input pads. Each 16K bit block is composed of two balanced 64 X 128 bit arrays sharing 128 sense amplifiers. Key aspects of the 64K dynamic RAM is summarized in Table I, in which typical DC supply voltages are 7 V for $V_{DD}$ and -2 V for $V_{SS}$. The memory cell yields a bit line capacitance ratio $C_B/C_G$ of about 7 in the present design.

Figs. 2A and 2B show the sense amplifier circuit and its simulated signal waveforms. This circuit is a variation of the simple cross coupled latch, which gives perfect dynamic operation. Two balancing transistors connect parallel with the cross coupled transistors, one another, and achieve early potential balance between a complementary bit line pair in reset mode. Although 80 mV is estimated as the worst case differential signal input, the memory cell gives a sense node difference of 170 mV to the bit line pair. No static current flow is observed in the sense amplifier circuit. During a typical read cycle, $t_{cycle}=400$ns, the 512 sense amplifiers dissipate approximately 60 mW which is less than 40 percent of the chip power.

Fig.3 shows waveforms of the 64K dynamic RAM, where $t_{access}$ and $t_{cycle}$ are 110 ns and 300 ns, respectively. The operating conditions are $T=25 \, ^\circ\mathrm{C}$, $V_{DD}=7 \, V$, $V_{SS}=-2 \, V$ in the marching test mode. The present channel-doped RAM (SAMPLE A) shmoo-plot shows wide supply-voltage-margin as shown in Fig.4 in comparison with that of SAMPLE B fabricated on highly impurity-concentrated substrate without channel doping. Other device features are shown in Table II. In conclusion, the present 64K RAM fabricated using channel-dope, short-channel technology has realized the wide operating range and high speed operation.
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Fig.1B Chip Layout.

Fig.2A Sense Circuit.

Fig.2B Simulated waveforms.

Fig.3 64K RAM Waveforms

Fig.4 64K RAM Shmoo Plot

Technology
Single Poly-Si Nch-MOS
Organization
16 kwords X 4 bits
Memory cell
1 Tr Cell
Cell size
15 μm X 18 μm
Chip size
4.72 mm X 7.05 mm
Supply voltage
7 V, -2 V
I/O levels
TTL (including RAS, CAS)
Address
Multiplexed address
Refresh
128 cycle / 2 ms

Table I. 64K RAM Characteristics

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<thead>
<tr>
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<th>Sample A</th>
<th>Sample B</th>
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<tr>
<td>Substrate Concentration</td>
<td>1 X 10^19 cm^-3</td>
<td>1.3 X 10^18 cm^-3</td>
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<tr>
<td>Gate oxide Film</td>
<td>400 Å</td>
<td>400 Å</td>
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<tr>
<td>Effective Channel Length</td>
<td>2μm</td>
<td>2μm</td>
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<tr>
<td>Threshold Voltage for Vp=1 V</td>
<td>0.85 V</td>
<td>0.95 V</td>
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<tr>
<td>Access Time</td>
<td>110 ns</td>
<td>150 ns</td>
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<tr>
<td>Cycle Time</td>
<td>300 ns</td>
<td>400 ns</td>
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<tr>
<td>Power Dissipation (at 400 ns cycle time)</td>
<td>&lt;150 mW</td>
<td>&lt;120 mW</td>
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<tr>
<td>Standby Power</td>
<td>&lt;15 mW</td>
<td>&lt;10 mW</td>
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Table II. Typical 64K RAM Features