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A-3-4 A High Speed I^2L 1K Static RAM with 20 ns Access Time

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A fully static I^2L 1024 × 1 bit RAM with access time of 20 ns was developed by introducing the improved I^2L memory cell structure.

I^2L memory cells[1][2], which are composed of lateral pnp and inversely operated npn flip-flop transistors, have been attractive for their high-density and low-power consumption capability.

The npn coupled I^2L memory cell[1], which is shown in Fig.1, has been known to give a fast read access time owing to the normally operated npn bit transistor. But it has a disadvantage of a longer writing time because only writing current divided by βd, where βd is the downward current gain of the bit transistor, is utilized to invert the flip-flop. It is necessary to reduce βd to improve the writing time. However, the inverse current gain βu of the flip-flop transistor should be larger than unity to keep the bistability of the flip-flop. Moreover, βu is desired to be as large as 2 ~ 4 to get a stable operation of the flip-flop. As βu/βd is usually 1/60 ~ 1/100 in the conventional I^2L structure, βd is not able to be reduced to a low value, which results in a poor writing time.

A new structure shown in Fig.2 was proposed to improve the writing time of the npn coupled cell. The bit transistor was fabricated by the doubly diffused base technology. βd of the bit transistor could be reduced by increasing the base width of the bit transistor without influencing βu of the flip-flop transistor. The higher βu/βd than 1/10 is easily obtained in the new structure.

To get the optimum value of βd, the read access time Tacc and the minimum write pulse width Twmin were measured with the new structure. The results were shown as a function of βd in Fig.3, together with the results in the conventional structure. Twmin could be improved by reducing βd. Though Tacc increases with reducing βd, the degradation of the read operation was not pronounced when βd is larger than 20. The optimized Tacc and Twmin could be obtained with the new structure cell by controlling βd to be 20 ~ 40.

A high speed I^2L RAM was realized by introducing the double diffused I^2L memory cell. Principal function blocks of this RAM were shown in Fig.4, where the peripheral circuits such as decoder, bit/word driver and sense amplifier were constructed by CML. The standby current of a cell could be decreased down to 3.5 μA.

The fully static 1K I^2L RAM operated at the address access time of 20 ns and

the minimum write pulse width of 50 ns with a power consumption of 350 mW and a single supply voltage of 5 V. Fig.5 shows an example of output waveform. The microphotogragh of the RAM chip with 3.96 × 3.96 mm^2 die area is shown in Fig.6.

[1] S. K. Wiedmann and H. H. Berger, Electronics, Feb. 14, pp.82-86, 1972.

[2] S. K. Wiedmann, in Dig. Tech. Papers, 1973 IEEE ISSCC, pp.56-57.

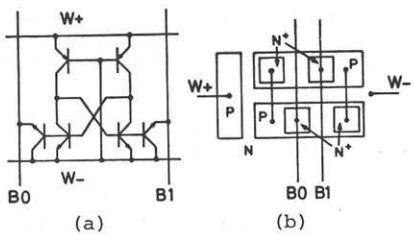

Fig.1 npn coupled memory cell.
(a) Equivalent circuit.
(b) Cell structure.

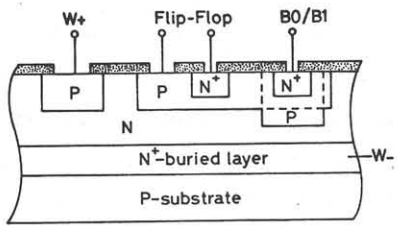

Fig.2 Cross section of the double diffused memory cell structure.

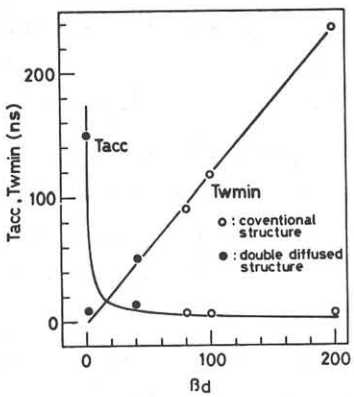

Fig.3 Tacc and Twmin versus βd of the bit transistor; read current is 100 μA and write current is 5 mA.

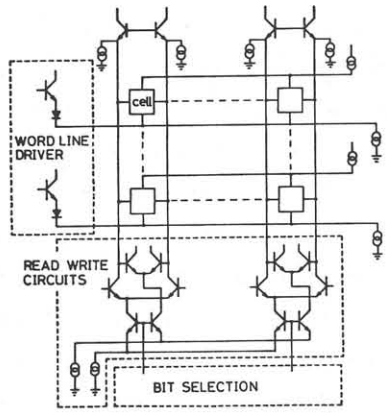

Fig.4 1K RAM schematic.

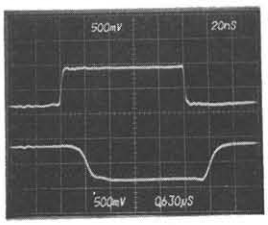

Fig.5 Output waveform showing access time of 20 ns.

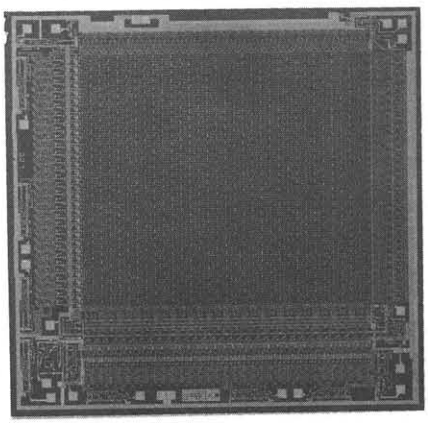

Fig.6 Microphotogragh of the chip; size is 3.96mm × 3.96mm.