A High Speed $I^2L$ 1K Static RAM with 20 ns Access Time

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A fully static $I^2L$ 1024 x 1 bit RAM with access time of 20 ns was developed by introducing the improved $I^2L$ memory cell structure.

$I^2L$ memory cells[1][2], which are composed of lateral pnp and inversely operated nnp flip-flop transistors, have been attractive for their high-density and low-power consumption capability.

The nnp coupled $I^2L$ memory cell[1], which is shown in Fig.1, has been known to give a fast read access time owing to the normally operated nnp bit transistor. But it has a disadvantage of a longer writing time because only writing current divided by $\beta d$, where $\beta d$ is the downward current gain of the bit transistor, is utilized to invert the flip-flop. It is necessary to reduce $\beta d$ to improve the writing time. However, the inverse current gain $\beta u$ of the flip-flop transistor should be larger than unity to keep the bistability of the flip-flop. Moreover, $\beta u$ is desired to be as large as 2 - 4 to get a stable operation of the flip-flop. As $\beta u/\beta d$ is usually 1/60 - 1/100 in the conventional $I^2L$ structure, $\beta d$ is not able to be reduced to a low value, which results in a poor writing time.

A new structure shown in Fig.2 was proposed to improve the writing time of the nnp coupled cell. The bit transistor was fabricated by the doubly diffused base technology. $\beta d$ of the bit transistor could be reduced by increasing the base width of the bit transistor without influencing $\beta u$ of the flip-flop transistor. The higher $\beta u/\beta d$ than 1/10 is easily obtained in the new structure.

To get the optimum value of $\beta d$, the read access time $T_{acc}$ and the minimum write pulse width $T_{wmin}$ were measured with the new structure. The results were shown as a function of $\beta d$ in Fig.3, together with the results in the conventional structure. $T_{wmin}$ could be improved by reducing $\beta d$. Though $T_{acc}$ increases with reducing $\beta d$, the degradation of the read operation was not pronounced when $\beta d$ is larger than 20. The optimized $T_{acc}$ and $T_{wmin}$ could be obtained with the new structure cell by controlling $\beta d$ to be 20 - 40.

A high speed $I^2L$ RAM was realized by introducing the double diffused $I^2L$ memory cell. Principal function blocks of this RAM were shown in Fig.4, where the peripheral circuits such as decoder, bit/word driver and sense amplifier were constructed by CML. The standby current of a cell could be decreased down to 3.5 $\mu$A.

The fully static 1K $I^2L$ RAM operated at the address access time of 20 ns and
the minimum write pulse width of 50 ns with a power consumption of 350 mW and a single supply voltage of 5 V. Fig.5 shows an example of output waveform. The microphotograph of the RAM chip with $3.96 \times 3.96$ mm$^2$ die area is shown in Fig.6.


(a) Fig.1 n-p-n coupled memory cell.
(b) Equivalent circuit.

(a) Cell structure.

Fig.2 Cross section of the double diffused memory cell structure.

Fig.3 Tacc and Twmin versus $\delta d$ of the bit transistor; read current is 100 $\mu$A and write current is 5 mA.

Fig.4 1K RAM schematic.

(a) Fig.5 Output waveform showing access time of 20 ns.

Fig.6 Microphotograph of the chip; size is $3.96 \times 3.96$ mm.