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Mo-gate MOS Metallization System

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Low resistivity and very fine patterning metallization system is required to make a high speed and high integration MOS LSI. Generally, poly-Si and aluminum (Al) are used for gate material and metallization, respectively. Mo has resistivity no greater than 1/100 that of poly-Si. Then Mo-gate technology is essential to develop 256K and/or further large MOS RAM. In the past, several MOS metallization systems[1,2] using a refractory metal-gate were proposed to overcome difficulty to reduce poly-Si resistivity or to make a fine pattern of Al. However, those attempts were not successful till recent times as there was an instability in MOS characteristics. The Mo-gate MOS metallization system was investigated using two levels of Mo metal for the following.

(1) Mo, different from Al, can be used for high temperature processes.

(2) Very fine patterning is possible as it has a fine fiber texture. Good ohmic contact is made onto a shallow P-N junction and electromigration is not observed.

An MOS LSI fabrication process we have established using Mo-gate MOS metallization system is as follows.

(1) Selective oxidation.
(2) Gate oxidation (HCl).
(3) Mo deposition and patterning.
(4) Source and drain formation by ion implantation.
(5) High temperature annealing.
(6) Deposition and patterning intermediate PSG film.
(7) Deposition and patterning 2nd level Mo.
(8) Deposition and patterning passivated SiO_2.

Mo films are evaporated by an electron beam gun. Very fine patterning method and characteristics of Mo-gate MOS devices were revealed to construct the system.

Fine patterning It is difficult to make a fine Mo electrode pattern in uniform width throughout 3" diameter of wafer with a conventional Mo etchant[3]. New step etching method was developed. At the 1st, the area to be etched of an Mo film is oxidized with a $K_3Fe(CN)_6$ solution. And at the 2nd step, the oxidized Mo is etched off by a $N(CH_3)_4OH$ solution. Fig.1 shows very small side-etching characteristics of an Mo electrode by using above two step method. The Mo electrode 1.0 μm wide is fabricated within the distribution of ± 0.1 μm. Fig. 2 shows a scanning electron micrograph of a 1.5 μm width Mo electrode on a PSG film with steps 0.7 μm high.

Characteristics of Mo-gate MOS Several important problems must be solved before a stable Mo-gate MOS devices are realized.

(1) Mo-gate does not have the passivation effect against mobile charge. Therefore, it is essential to make a contamination-free gate process. In the Mo-gate, mobile charge contamination occurs in the process of Mo film evaporation and photolithography. Contamination has been prevented by using Mo evaporation apparatus, with which a contamination-free process is possible, and by washing in a H_3PO_4 solution. Contamination-free annealing technology has been established by developing an instrument, with improved ambient gas control in which Mo is not oxidized. Mobile charge density of Mo-gate MOS devices is less than $1 \times 10^{10}/cm^2$.

(2) When an Mo film was evaporated, large surface state and surface charge

density were produced. However, they were extinguished by improving evaporation technique and annealing above 1000°C in nitrogen and at 450°C in hydrogen atmosphere. Surface state and surface charge density is now reduced to 2 x 10^{10}/cm^2eV, 5 x 10^{10}/cm^2, respectively. Fig.3 shows flat band voltage (V_{FB}) and dielectric breakdown field (E_g) on high temperature annealing. V_{FB} was raised to - 0.3 V and was stabilized there. E_g was not decreased by the annealing. Stability of Mo/SiO_2 structure was investigated with Auger electron spectroscopy. Mo was not observed in SiO_2film after Mo/SiO_2 was annealed at 1000°C. Further, Mo/SiO_2 interface was confirmed to be stable for MOS process including high temperature annealing.

Table I shows characteristics of Mo/SiO_2 structure in the devices made by the established Mo-gate process. The decrease of channel mobility is little for the decreased effective channel length. Fig.4 shows threshold voltage (V_{th}) distribution of Mo-gate MOS transistors. The V_{th} deviation of MOS transistor is very small (±0.025V). The change in the V_{th} was less than 0.05 V after B-T stress (bias stress : 1.8 x 10^6V/cm, ambient temperature : 200°C and stress time : 63 hours).

A high speed 16K MOS RAM[4] was made using this Mo-gate MOS metallization system. Access time of the devices is 65 ns. It is much smaller than that of same MOS RAM with Si-gate.

References

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2) R.C. Henderson, et al.: IEEE J. Solid-state Circuits, SC-10, 92(1975).
3) D. M. Brown, et al.: J. Electrochem. Soc.,114, 730(1967).
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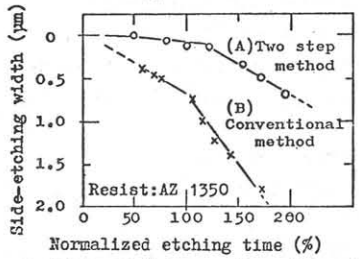

Fig.1 Side-etching value dependence on etching time.

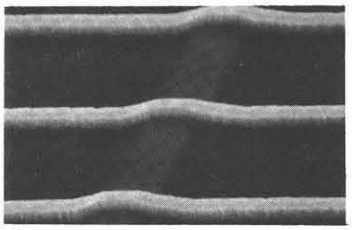

Fig.2 Mo electrode scanning electron micrograph.

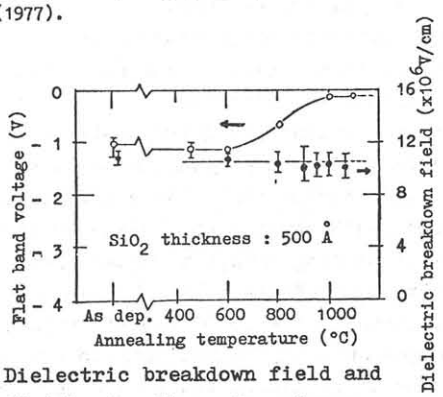

Fig.3 Dielectric breakdown field and flat band voltage dependence on high temperature annealing.

Table I Characteristics of Mo-gate MOS metallization system.

Resistivity	1 x 10^{-5}Ω·cm *)
	2.8 x 10^{-5}Ωcm **)
Contact resistance	1.2 x 10^{-6}Ωcm^2
Work function	4.7 eV
Flat band voltage	- 0.3 V
Surface state density	2 x 10^{10}/cm^2·eV
Fixed surface charge density	5 x 10^{10}/cm^2
Mobile charge density	1 x 10^{10}/cm^2
Channel mobility ***)	600 cm^2/V·sec

*) After 1000°C anneal, **) as deposit,
***) effective channel length : 2 μm.

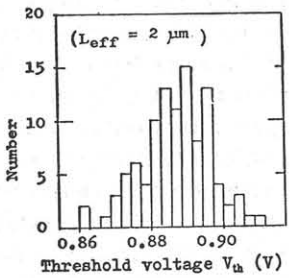

Fig.4 Threshold voltage distribution of Mo-gate MOS transistors.