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Application of High Current Arsenic
Ion Implantation to Dynamic MOS memory LSI's

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Arsenic ion implantation has been used for the fabrication of bipolar transistor emitters¹⁾ as well as MOS LSI source and drain regions²⁾. This is because of its attractive controllability and reproducibility features, although dense crystalline defects up to 10^9 cm^{-2} have been observed³⁾.

This paper presents the defect depth profile in relation to carrier profile. It also provides information on the electrical characteristics of the arsenic implanted layer, e.g. junction leakage current, dynamic MOS memory refresh time.

A high current ion implantor is used for the fabrication. Typical ion current is around 2 mA. The substrate is found to be cooled through radiation. Consequently, the temperature is less than 150°C under these implantation conditions.

The residual defect depth profile is measured by transmission electron microscope (TEM; Hitachi HU 12 A) utilizing the controlled layer removal method. Typical results are shown in Fig. 1, in which arsenic ions are implanted through a 50 nm thick silicon dioxide layer to a dose of $2 \times 10^{16} \text{ cm}^{-2}$ at a 120 keV accelerating energy. The annealing conditions are 1000°C in dry nitrogen atmosphere for 60 min. The dense dislocation region is found to be within 0.1 μm of the surface. The defect density is more than 10^{15} cm^{-3} as shown in Fig. 2, which might affect the carrier conduction as scattering centers. Therefore, the corresponding carrier profile is measured by the incremental sheet resistivity method. The results are shown in Fig. 2. These results clearly establish that the heavily damaged surface region has no effect on carrier conductivity. Although oxygen knock-on phenomena cause the dense dislocation formation⁴⁾, annealing in a non-oxidizing atmosphere is found to suppress dislocation propagation into the substrate. Therefore, dislocations might not affect junction characteristics.

Arsenic implanted layer is evaluated from the junction leakage current and the dynamic memory refresh time viewpoint. The devices used for evaluation are junction diodes (1 mm^2 area) and 4 K bit MOS memory LSI's (1 MOST / cell type; 20 μm^2 junction area). Junction leakage current is in the order of $10^{-10} \text{ A} / \text{cm}^2$ at room temperature at 10 V reverse bias, indicating a 10^{10} cm^{-3} generation-recombination center concentration in the depletion region.

Memory refresh time is measured between 40 and 90°C. The mean value of the

integrated fail bit proportion and refresh time relationship is shown in Fig. 3. The mean refresh time at 70°C is 140 ms, and the deviation is 20 ms. The activation energy above 70°C is 1.1 eV and below, 0.55 eV. These results coincide well with the leakage current measurements.

These electrical characteristics clearly indicate that defects generated by heavy arsenic ion implantation have no effect on device characteristics.

references

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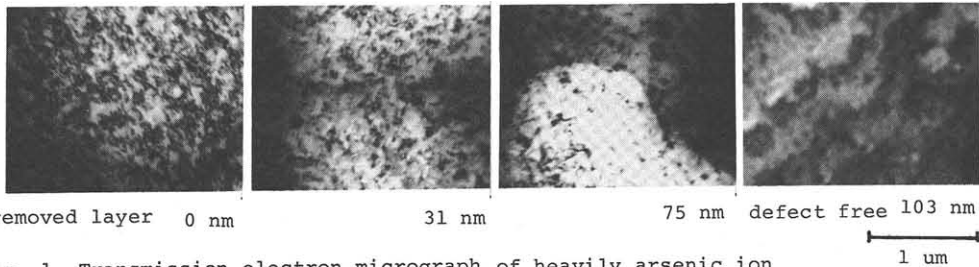


Fig. 1 Transmission electron micrograph of heavily arsenic ion implanted layer; layer removal method

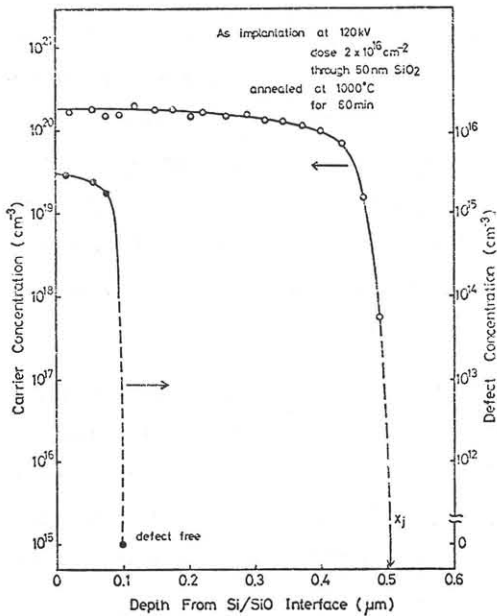


Fig. 2 Defect and carrier depth profile; corresponding to Fig. 1

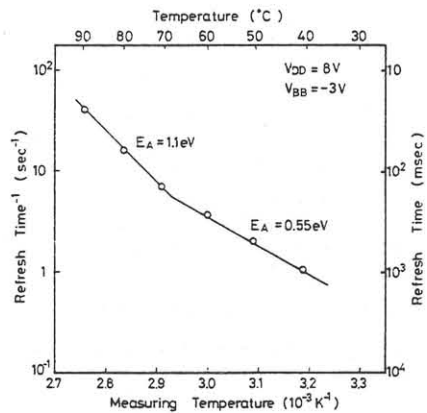


Fig. 3 Temperature dependence of memory refresh time