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A−4−3 Selective Oxide Coating of Silicon Gate (SELOCS)

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Decreasing the thermal oxidation temperature of silicon in wet oxygen is known to enhance the impurity concentration dependence of the oxidation rate. The entire surface of phosphorus doped polysilicon gate has been uniformly covered with its own oxide utilizing such concentration dependent oxidation.[1)] This technique has been named SELective Oxide Coating of Silicon gate (SELOCS).[2)] Phosphorus concentrations greater than $1x10^{20}cm^{-3}$ have been found to cause an increase in oxidation rates. However, oxidation rates tend to saturate above $1x10^{21}cm^{-3}$. Typical oxidation rates of $700nm^2/min$ and 0.5nm/min are obtained for phosphorus concentrations of $1x10^{21}$ and $1x10^{20}cm^{-3}$, respectively, at 750°C.[3)]

The SELOCS process sequence particularly appropriate for the fabrication of fundamental MOS transistors is shown in Fig. 1. A cross-sectional view of SELOCS structure corresponding to d) in Fig. 1 is shown in Fig. 2. This is obtained by 850°C wet oxidation, uniform etch back by DUE process (described later) and As implanted polysilicon metallization. Fundamental electric characteristics of this transistor are satisfactory and displays no difference from those of conventional silicon gate transistors.

One key to realization of the SELOCS MOS transistor is the etch back process. Conventional SiO_2 etchants, e. g. HF buffered solution, may not produce a sufficient break down voltage in the intermediate polysilicon oxide due to anomalous etching of the oxide around gate edges. A DUE (Diffusion defined Uniform Etching) process is introduced to realize uniform etching of the oxide. This process utilizes the uniform formation of PSG film on the oxide surfaces by a predeposition with a $POCl_3$ source. The PSG film is subsequently removed by P-etchant[4)] which selectively attacks phosphorus contained SiO_2. Typical breakdown voltage distribution is shown in Fig. 3. The distribution is

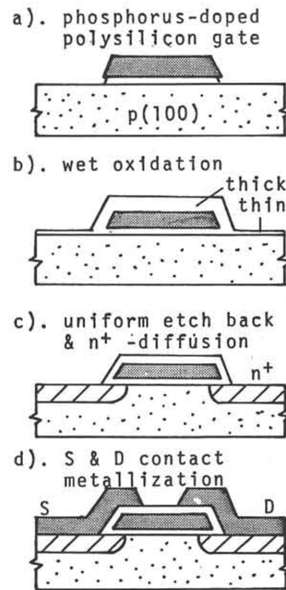
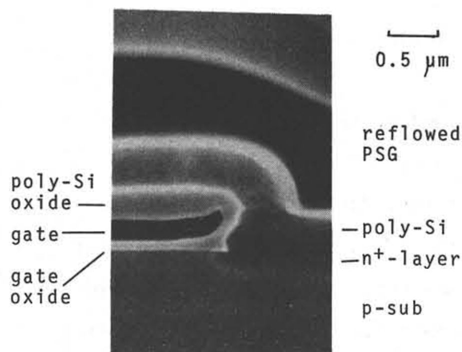


Fig. 1 Process sequence for a fundamental MOS trs. using SELOCS technique.



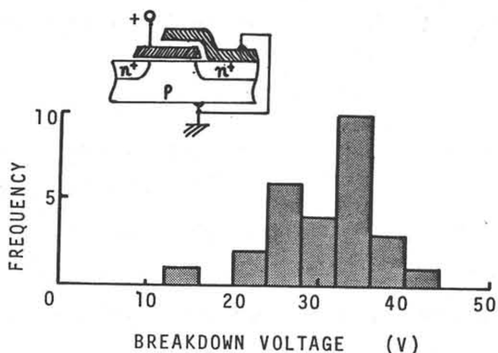


Fig. 2 Scanning electron micrograph of a typical SELOCS structure cross-section.

Fig. 3 Breakdown voltage distribution for a typical MOS transistor structure.

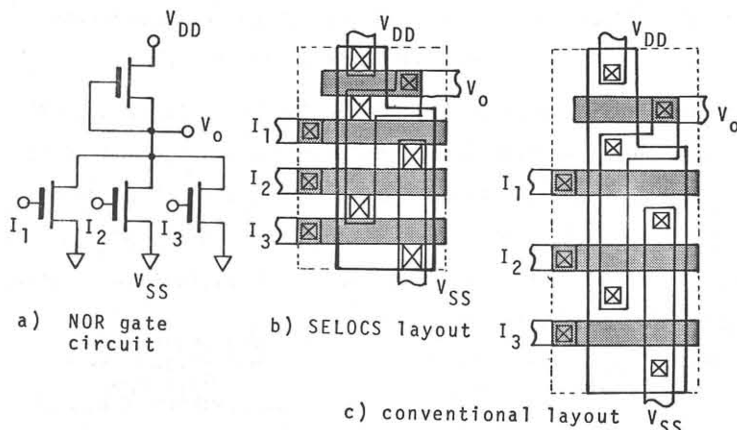


Fig. 4 A comparison of SELOCS and a conventional rule for a typical 3 input-NOR gate. (5 μm rule technology)

scattered to some extent. Some improvement of the oxide formation is still required, though experimental data show no shortage.

One of the most important advantages of SELOCS is the definite zero registration tolerance between the photoengraving of contact holes to S & D and the polysilicon gate. This is because contact hole definition is one main obstacle hindering area reduction in today's LSI's. SELOCS can provide a reduction ratio of around 2 without requiring finer pattern lithography. A comparison of layout patterns by SELOCS and a conventional rule according to 5 μm-rules is shown in Fig. 4 for a typical 3 input-NOR gate. In addition, this technique can readily be applied to double, or more level, polysilicon devices, e. g. MOS memories, CCD's.

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