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A-5-4 Application of IPOS technique to MOS IC

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IPOS (Insulation by oxidized POrous Silicon) technique has been investigated for isolation in MOS ICs. By IPOS technique,[1] in which silicon is anodized in hydroflouric acid to make porous silicon and oxidized, thick SiO_2 film can be obtained in short oxidation time because the oxidation rate of the porous silicon is very fast. Besides the IPOS technique has other advantages such that the thick SiO_2 film is recessed in Si surface and doesn't make a step.

We developed the IPOS technique for MOS IC in which leakage current of reverse biased pn junction must be extremely small. The availability of the IPOS technique for MOS process was confirmed by the application to 1 kbit MOS RAM.

To form the oxidized porous silicon selectively, Si_3N_4/SiO_2 structure is used as a mask for anodic reaction and oxidation.

Figure 1 shows the reverse I-V characteristic of pn junction using the different HF acid concentration in anodic reaction. The leakage current in the case of 35 % HF acid was found to be extremely smaller than that in the case of usually used 50 % HF acid. To investigate the defects which cause the leakage current, sample wafers were etched in Wright etchant as shown in Figure 2.

The stacking fault density is far less in the case of 35 % or less than in the case of 50 %. Figure 3 shows the density of porous silicon vs. the HF acid concentration in anodic reaction. The value of density, 1.0 g/cm^3 at 35 % HF is just the value that the oxidized porous silicon fills the volume that the porous silicon have before it is oxidized. If the HF concentration above 35 % is used, the expansion of the oxidized porous silicon causes the lattice strain. Figure 4 shows the SEM cross sectional view of the IPOS structure. The step height is as small as 0.1 μm.

A 1 kbit dynamic MOS RAM was fabricated using the IPOS technique. Figure 5 shows a photograph of whole chip. Pattern rule of 2 μm minimum width is used in this RAM.

The reduced leakage current has made dynamic operation possible and the small width (3.5 μm) of isolation is applicable for the high density RAM.

Reference

1) Y.Watanabe,Y.Arita,T.Yokoyama and Y.Igarashi J.Electrochem. Soc.,122, 1351 (1975).

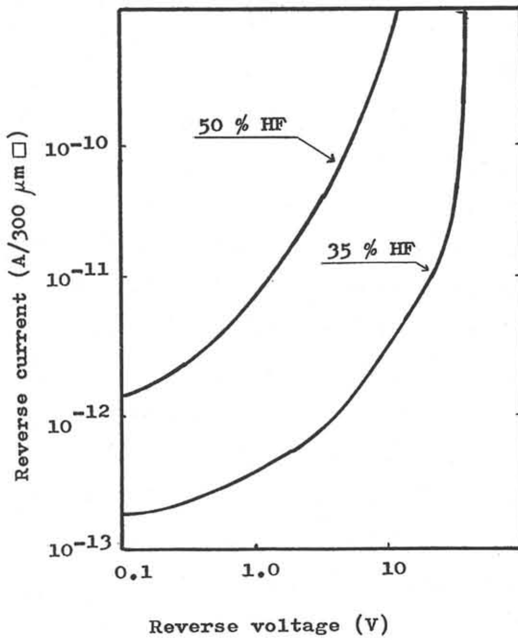

Fig.1 Reverse I-V characteristic

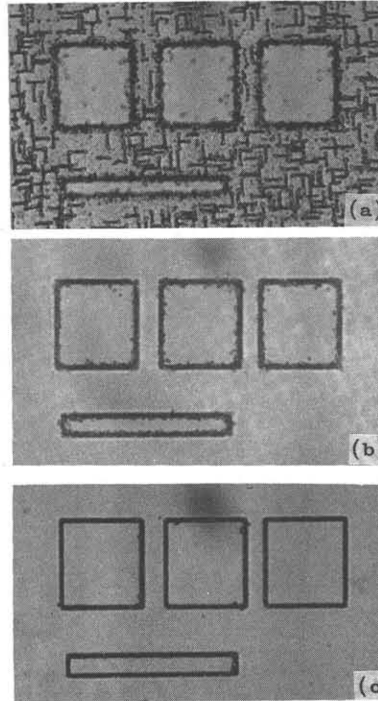

Fig.2 Silicon wafer after 60 sec etching in Wright etchant
(a) 50 % HF (b) 35 % HF
(c) 25 % HF

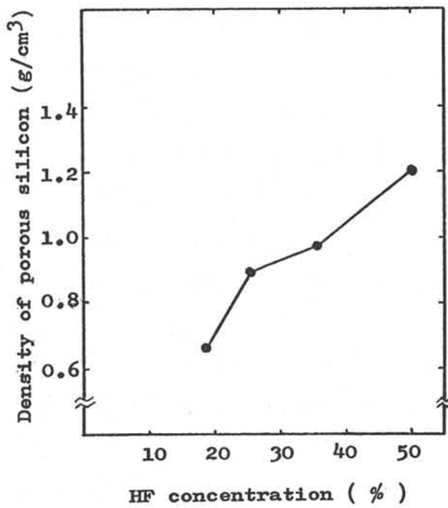

Fig.3 Density of porous silicon vs. HF concentration

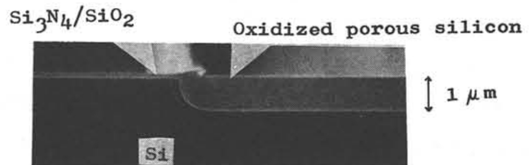

Fig.4 SEM cross sectional view

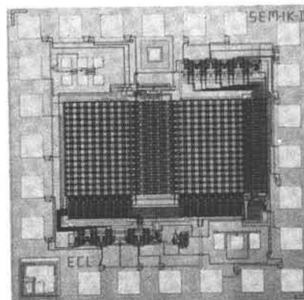

Fig.5 1k Chip Photograph