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A－6－1 (Invited) Electron Beam Lithography in Practical Use for Integrated Circuits

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Along the rapid development of integrated circuits technology, electron beam lithography has increasingly been necessiated, because of its principal capability of high-resolution and fast pattern generation and of its potential flexibility. Currently the electron beam machines are expected to fabricate most efficiently master masks or reticles for advanced LSI's of feature size down to 2 or 1μm range. Most of the machines designed for practical use are aiming at a delineation time of one hour or less for 100×100mm substrate. For the pattern printing on wafers, the use of one-to-one or reduction-type projection aligners is believed to be a realistic solution in the range down to, say, 1.5μm in coming a few years. The direct electron beam writing on wafers is also possible by the currently available electron beam machines for limited purposes. The direct electron beam exposure system for real VLSI's in submicron range will remain to be explored in several years to come.

In this paper we discuss some key problems to achieve high-resolution patterning and fast delineation of advanced LSI's. Since a higher density and a higher resolution patterns directly mean a larger amount of pattern data, the problems relate in particular to the data processing system, the electron optical system, the electron resists and wafer fabrication process. For the high-resolution patterning, a large amount of data processing, fine electron beam spots and high resolution resists are inevitable. Delineation speed is limited by data rate, current density and electron resist sensitivity. High resolution and fast delineation are somewhat ambivalent about the design of practical electron beam exposure system. The total system of electron beam lithography should be optimized over these key parameters.

For all the machines, sensitive, productive and reliable electron resists are urgently required. At present, PMMA is said to be most practical among many positive resists, but it requires electron dose more than $10\mu C/cm^2$. To realize the high dose with small beam spots, it is necessary to get high current density with least sacrifice of the delineation speed.

An electron beam exposure system, VL-R1, which is of a raster-scan type with moving workstage, has been developed. Details of this machine will be published

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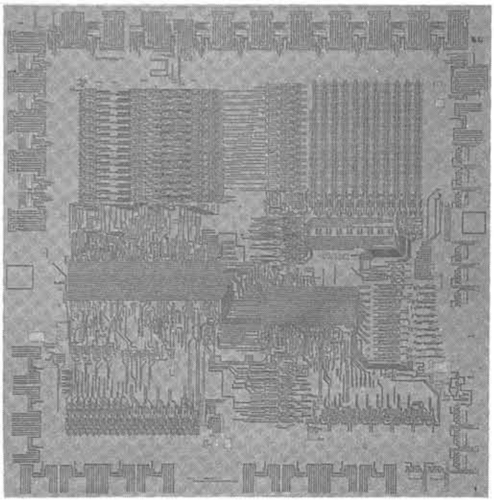
*Present address: Toshiba Research and Development Center, Komukai, Kawasaki elsewhere, but an outline and some experimental results will be given here from above-mentioned stand points. VL-R1 is providedby a 160MB magnetic disk, a specially designed DMA and data compaction function to process a large amount of data with transmission rate of 20Mbit/sec. Providing a LaB_6 cathode and a short working distance in electron optical column, current density of more than $300A/cm^2$ is obtained. This current density enables us to expose PMMA resist.

Evaluating a total performance of VL-R1, we delineated a model pattern of a 16-bit minicomputer CPU of 1μm geometry as an example of high-density LSI's at a speed of 1sec/chip on a PMMA resist substrate. The pattern data were derived by scaling down of its original pattern of 6μm geometry on a 5.5×5.5mm chip. A microscopic photograph of the developed pattern is given in Fig. 1. Best parameters concerning the delineation condition for PMMA as an electron resist will be presented. When new practical resists of higher sensitivity with high-resolution than PMMA are developed, VL-R1 is capable of increasing the writing speed up to the limit of its data rate.

In addition to the pattern resolution and delineation speed, any practical electron beam machine should be deliberately designed to have enough accuracy and stability. Conciderin g any types of the electron beam exposure systems, including even a VSB scheme, which is a promissible one of next-generation machines, optimization of data processing system, electron optical system and electron resists would be most important for the high-resolution patterning and the fast delineation of high-density LSI's.



0.92 × 0.92mm

Fig. 1. A resist pattern of a model 16-bit CPU of 1μm geometry.