Digest of Tech. Papers The 10th Conf. on Solid State Devices, Tokyo

A-6-2 Direct Electron Beam Data Writing Technology for 128K EB-ROM

E. Arai, T. Ogawa, N. Ieda, K. Kiuchi, K. Iwadate, and K. Takeya
Musashino Electrical Communication Laboratory, NTT
Musashino-shi, Tokyo 180 Japan

A 128-kbit MOS read-only memory (MOS EB-ROM) has been developed using direct electron beam data writing and advanced technologies. The direct electron beam writing technology has advantages in providing a very high degree of pattern flexibility and shortening the turn around time of LSI fabrication. Taking these advantages into account, the technology has been applied to data writing of 128K ROM, based upon new techniques such as 1) scanning electron beam exposure system, EB-50 developed at Musashino Electrical Comm. Lab., with high registration accuracy, 2) advanced wafer processing steps to match electron beam lithography, 3) highly sensitive positive type resist, FPM developed at Ibaraki Electrical Comm. Lab., with typical sensitivity of $6 \times 10^{-6} C/cm^2$.

To realize the high integration ROM, it is necessary to minimize memory cell size and delay time in the interconnections. The small cell size of $8 \mu m \times 7.75 \mu m$ is realized by reducing the number of contact holes to 0.5/bit. Programming information in the array has been achieved by selecting the devices in the array, whose threshold voltage is modified by using field oxide as a gate oxide in place of thin gate oxide. Word lines, bit lines and current return paths consist of polysilicon, second layer metal (Mo) and diffused layer, respectively. The memory cell array is divided into 4 blocks to lower the delay time and to make pattern layout easy. The 128K ROM is organized as a 16 Kword x 8 bit format. A blockdiagram of the ROM is shown in Fig.1. Moreover, to obtain low power dissipation and TTL compatibility, advanced circuit technologies with E/E dynamic inverters and a single supply voltage are employed.

The processing steps for data writing by EB lithography are shown in Fig.2. The 1st level patterning is divided into 2 steps. First, the whole diffusion and transistor areas are defined by photolithography and, subsequently, some transistor gate areas in memory cells are exposed by EB lithography according to the information to be stored, for Al film evaporated on CVD Si_3N_4. The Al film is etched off by plasma etching with CCl_4 gas, using AZ1350J resist for photolithography and FPM resist for EB lithography. The produced Al patterns are used as a registration mark for EB lithography and as a mask for plasma etching of CVD Si_3N_4 film and for boron ion implantation.

Direct electron beam data writing has been carried out by EB-50 with 5 MHz maximum beam stepping rate and 2 mm x 2 mm deflection field size, where pattern

dimensions written in the cells are 1.5μm x 5.5μm rectangles. The ROM chip of 5.5 mm x 3.75 mm is obtained by stitching a 3 x 2 array of 1835μm x 1875μm subfield. For resistration, deflection errors are measured and compensated by scanning beam over a gold calibration grid, This compensation has been effective during 7-day operations. The wafer rotation alignment is executed using a pair of Al marks separately placed on a wafer. Field shift correction is subsequently carried out by detecting a cross shaped Al mark 10μm wide in a corner of each chip. It is difficult to strip the overexposed resist caused by beam scanning on the mark. To accomodate the resist stripping, bidirectional raster scanning for mark detection is used. A typical mark detection signal is shown in Fig.3.

FPM resist 1μm thick is spincoated on wafers, where exposure codition of 2×10^{-5} C/cm^2 is selected in the present work. Writing time is 2 minutes per chip at 1.3 MHz stepping rate and 1 nA beam current. The alignment accuracy of ± 0.18 μm and the resist pattern size accuracy of ± 0.15μm have been achieved through the present work. The other processing steps consist of improved 64K fabrication process with 2μm minimum pattern width.[2)]

The fabricated EB-ROM is capable of 200 ns access time and 65 mW power dissipation for 400 ns cycle time. A microphotograph of the chip is shown in Fig.4. Key device characteristics are summarized in Table I. The ROM is loaded with Chinese ideograph patterns and is tested in a Chinese ideograph display, where a memory capacity of 288 bits per character is necessary to memorize the shape of a Chinese ideograph.

References 1) K.Murase et al.: Tech. Papers of inter. conf. on microlithography ('77, Paris) p.261. 2) E.Arai et al.: Digest of tech. Papers of ESSCIRC '77 p.74.

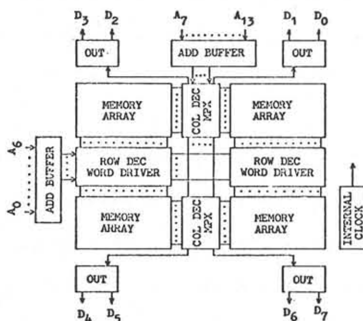

Fig.1 Block diagram of 128K EB-ROM.

WORD ORGANIZATION	16kword x 8bit
ACCESS TIME	200 ns
CYCLE TIME	400 ns
POWER DISSIPATION	65mW
DC SUPPLY	+5 V
CELL SIZE	62 μm^2
CHIP SIZE	20.6 mm^2

Table I Summary of the device characteristics.

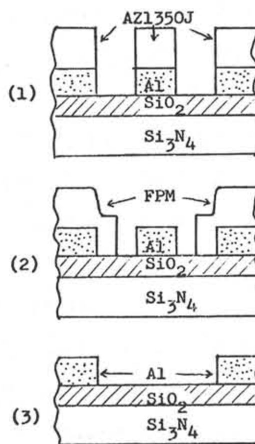

Fig.2 Processing steps of data writing.

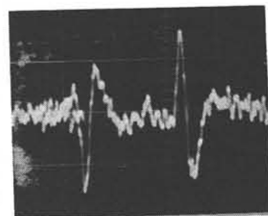

Fig.3 Mark detection signal for registration.
(Al thickness:0.35 μm)

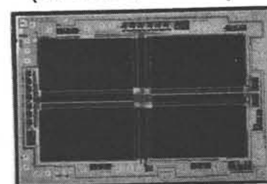

Fig.4 Photograph of 128K EB-ROM.