A－6－4 MOS LSI Fabrication Process Using Direct Electron Beam Writing

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MOS LSI fabrication process using direct electron beam writing has been developed and has been applied to fabricate the 1k MOS RAM with a minimum pattern dimension of 2μm.

Optimum exposure conditions for positive resist PMMA are determined to obtain undercut resist profile for lift-off and accurate line width, considering the proximity effect and resist thickness dependence. To satisfy the requirement for both undercut profile and line width for single line, dose range is limited to $1.5\text{-}3.3\times10^{-4}C/cm^2$ as shown in Fig.1. Figure 2 shows changes of exposure intensity distribution at various points along 2μm-wide single line, due to intra-proximity effect. Optimum dose for undercut profile at every point is obtained in the above mentioned dose range. No correction for proximity effect is necessary for 2μm-rule LSI patterns in this case. The relation between resist thickness and optimum dose is important, because resist thickness varies with surface steps. This relation is determined by the developing characteristics of resist, and is not critical for PMMA, as shown in Fig.3. Thickness of Al will be limited for finer line width, because the shape of remained Al in lift-off step is tapered by the growth at the side of Al on the resist.

Amounts of oxide trapped charges and fast surface states induced by EB irradiation are sensitive to the gate oxidation process. Dry O_2 oxidation at 1000°C was selected because of less sensitivity compared with higher temperature oxidation. The damage in two typical writing stages i.e. patterning of gate electrode and 2nd level electrode has been studied. For the gate electrode where the $Si\text{-}SiO_2$ interface is irradiated through polysilicon and PMMA resist, induced oxide charge density of $1\times10^{12}cm^{-2}$ just after irradiation of 20 keV EB with a dose of 2×10^{-4} C/cm^2, is almost eliminated by annealing above 700°C. For the 2nd level electrode where the annealing temperature is limited to about 500°C because of the metal-silicon reaction, the smaller amount of trapped charge is induced, and is annealed out by the lower temperature heat-treatment at about 450°C. Fast surface states created in both stages are easily annealed out by the heat-treatment at 400-500°C.

The basic processing steps are shown in Table I, and are based upon 64k RAM process[1] except for lithography. Even after removal of Al mask, residual Al atoms on Si_3N_4 and polysilicon surfaces were detected by SIMS analysis. In order to avoid Al contamination, thin oxide layers are grown on those films prior to Al

deposition and are etched off after Al removal. The optimum plasma etching conditions for such double-layered structures are attained by controlling oxygen concentration in reactant gas (CF_4-O_2). PMMA was used as a mask for contact hole etching of PSG with buffered HF. Postbake at 135°C gives good adhesion between PMMA and PSG and little geometrical change in resist shape. Accurate patterning of Mo is realized by wet chemical etching with the solution made of $K_3[Fe(CN)_6]$, $(NH_4)_2C_2O_4$ and H_2O which scarcely etches Al mask (Fig.4).

Applying the mask transfer process developed and optimizing the processing schedules to anneal out radiation damage, the 1k MOS RAM has been produced. Characteristics, such as hold time and FET threshold voltage, are the same as those of devices fabricated by photolithography. The outlook in the satisfactory chip yield has been obtained by utilization of the accurate resist pattern generation and mask transfer processes. 1) E.Arai and N.Ieda: Digest of tech. Papers of ESSCIRC '77 p.74.

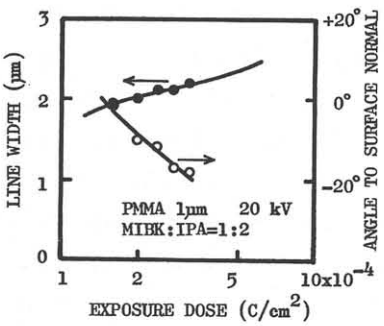

Fig.1 Variation in line width and angle of developed line edge with exposure dose for 2 μm-wide designed line.

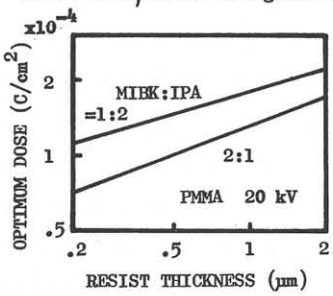

Fig.3 Variation in optimum exposure dose with resist thickness.

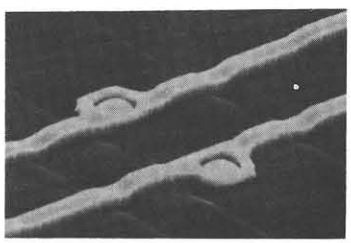

Fig.4 Scanning electron micrograph of memory cells.

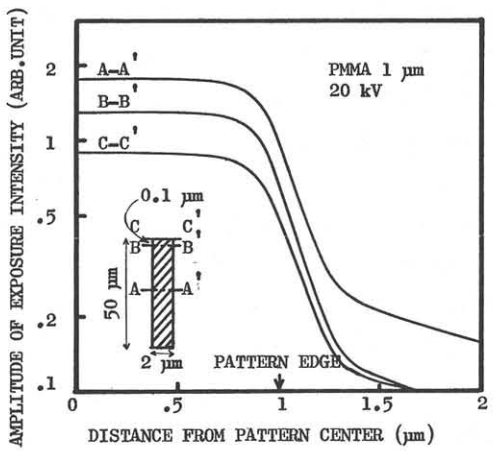

Fig.2 Exposure intensity distributions simulated using experimentally obtained single-spot-line distribution.

Table I. Processing Steps

Device area definition (1st writing level)	Al lift-off, plasma etching of Si_3N_4 and B implantation with Al mask, selective field oxidation
Gate electrode definition (2nd writing level)	Al lift-off, plasma etching of polysilicon, As implantation (source and drain)
Contact hole definition (3rd writing level)	Flowed PSG, wet etching of PSG
Second layer metal definition (4th writing level)	Al lift-off, wet etching of molybdenum
Contact hole definition (5th mask level using photolithography)	Wet etching of PSG
Pad definition (6th mask level using photolithography)	Wet etching of Al