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A 380^H x 488^V CCD Imager with Narrow Channel Transfer Gates

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Introduction A new electrode structure for two-phase CCD has been[(1)] proposed. The built-in directionality is achieved by narrowing the transfer channel(s) of each electrode. The feasibility of this new structure has been confirmed in a 242 element analog delay line and the application is now extended to a $380^H \times 488^V$ CCD Imager. In the constructed B/W CCD camera, the horizontal image resolution of 280 TV lines per picture height has been obtained.

Device Structures and Fabrications The device has been organized for a frame transfer CCD. It consists of 380 x 244 bit imaging area, 380 x 244 bit storage area, and 380 bit horizontal readout shift register. In the imaging area, an SiO_2 exposed photo-sensor window of 21μm x 6μm is located in the CCD unit cell of 24μm x 14μm. Fig.1-3 show the photograph of the device, the unit cell of the imaging area, and the horizontal readout shift register. The chip size of the device is 10.1mm x 14.6mm in which the imaging area is 8.8mm x 6.6mm determined by 2/3-inch picture format of the optical system.

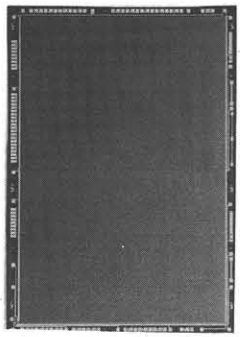
The device is fabricated in buried-channel version on a P-type (100) oriented, 10－20 ohm-cm silicon substrate with double-layer overlapping polysilicon gate definitions. The gate oxide thickness is 130nm throughout the device. Phosphorus doped polysilicon with the sheet resistivity of 50-70 ohm/□ and the thickness of 500nm is used for the gate electrode structure. To eliminate oxidation-induced stacking faults and other generation-recombination centers, high density (more than $1 \times 10^{20}/cm^3$) phosphorus gettering at 1100°C and HCl oxidation were employed. The typical dark current level is less than $5nA/cm^2$.

Imager Characteristics The transfer efficiency of the vertical and horizontal shift registers are more than 99.995% per transfer. And high image resolution of 280 TV lines/p.h.(Horizontal) and 350 TV lines/p.h.(Vertical) have been obtained. See Fig.4-5. Operating conditions of the CCD imager are as follows:

Integration Time	16 msec
Vertical Clock Voltage	from -2 volt to -12 volt
Frame Shift Frequency	14.31818 MHz/32=447.4 KHz
Line Shift Frequency	15.7 KHz
Horizontal Clock Voltage	from 3 volt to -12 volt
Readout Frequency	14.31818 MHz/2=7.15909 MHz
Interlace	2:1

The dark current level is less than 3% of the maximum signal level at the room temperature of 20°C. The spectral response of the imager is also analyzed and reported in Fig.6. It is expected that this inherently SiO_2 exposed structure has high enough quantum efficiency at 450nm wavelength and functions as a color imager with high sensitivity and resolution if the smearing problem, assosiated with the frame-transfer organization itself, is solved by use of a mechanical shutter.

Reference (1) Yoshiaki Daimon-Hagiwara, "TWO PHASE CCD with Narrow-Channel Transfer Regions", Proc. of the 9th Conf. on Solid State Devices, Tokyo, 1977; JJAP, Vol 17 (1978) Supplement 17-1, pp.255-261.



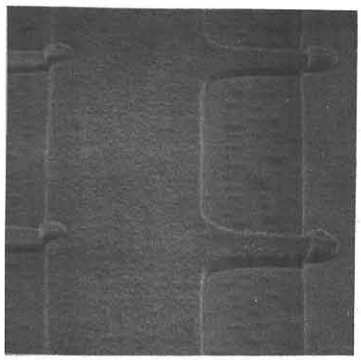


Fig.1 A $380^{H} \times 488^{V}$ CCD Imager with Frame Transfer Organization

Fig.2 SiO_2 exposed photo-sensor window of 21μm x 6μm located in the unit cell of 24μm x 14μm. The width of the narrow transfer channel is 3μm throughout the device. The electrode-overlap is 2μm.

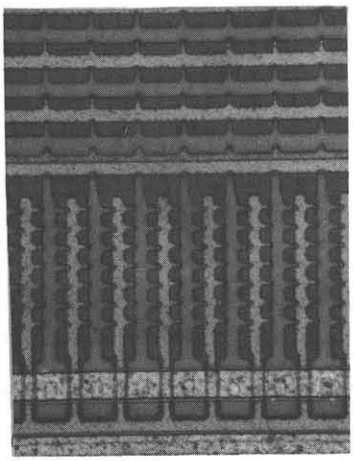


Fig.3 The horizontal readout register with 24μm-pitch-per-bit electrode structure

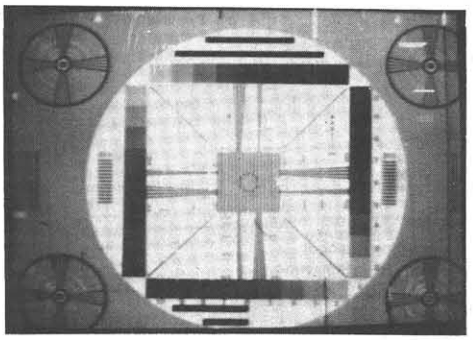


Fig.4 A TV picture of a resolution chart

Fig.5 A TV picture of an image

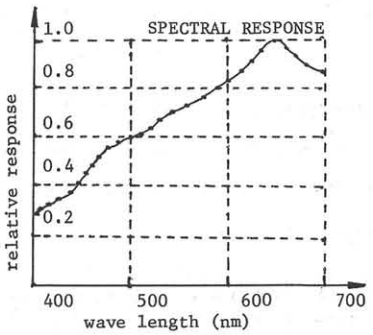


Fig.6 Spectral Response of the photosensors. Effective window size are 24μm x 14μm at 700nm and 21μm x 6μm at 400nm. Measurements were performed by reading the signal output of the imager while imaging a monocromatic spot light.