B－2－2 GaAs Integrated Logic with Normally-Off MESFETs

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The development of normally-off GaAs MESFET[1] digital integrated circuits with power consumption as low as 0.2 mW per gate and sub-nanosecond delay time are reported.

The basic logic circuit used in the IC's is a 2-input NOR gate consisting of two normally-off FETs and a load resistor. The circuit is fabricated on an n-GaAs layer grown onto a semiinsulating GaAs substrate. The doping density and thickness of the n-layer is 1×10^{17} cm^{-3} and 0.1 μm, respectively. The individual FET and load resistor are isolated each other by mesa steps and are interconnected by dual layer metal system. The space between source and drain of the FET is 5 μm. The length and width of the gate are 1.2 μm and 20 μm, respectively. The load resistor is 10 μm wide and 40 μm long.

Typical electrical parameters of the FET are; $g_o(max)$ = 1 mS, $I_D(max)$ = 0.8 mA, and V_T = +0.1 V where g_o, I_D, and V_T are the channel conductance at low drain voltage, saturated drain current, and threshold voltage, respectively. The load resistance is 8 KΩ.

To investigate the speed-power performance of the IC's, a 13-stage ring oscillator has been built and tested. Figure 1 shows a microphotograph of the test circuit consisting of a 13-stage inverter chain and an output buffer. The ring oscillator can be easily built by coupling the input and output pads of the inverter chain with a bonding wire. The propagation delay, t_{pd}, and the power-speed product, Pt_{pd}, of the ring oscillator are plotted each as a function of the supply voltage, V_{DD}, in Fig. 2. t_{pd} decreases with increasing V_{DD} while Pt_{pd} increases with V_{DD}. The achieved minimum propagation delay was 170 ps with Pt_{pd} = 120 fJ at V_{DD} = 3 V. The lowest power-speed product was 7.6 fJ with t_{pd} = 385 ps and V_{DD} = 0.6 V.

A binary frequency divider has been designed with a master-slave flip-flop. As shown in Fig. 3, the circuit consists of eight NOR gates and two buffer amplifiers. The maximum counting frequency was 610 MHz with the supply voltage of 1.5 V. This datum corresponds to the propagation delay per gate of 410 ps and power-speed product of 85 fJ.

For further reduction of the power-speed product, the gate width has been reduced to 10 μm keeping other parameters same. The experimental results on a

13-stage ring oscillator are shown in Fig.4. The minimum power-speed product of 2.3 fJ was obtained at V_{DD} = 0.4 V with t_{pd} = 500 ps, corresponding to the power consumption of 4.6 μW per gate.

In conclusion, the GaAs integrated logic with normally-off MESFETs is substantially feasible for high-speed LSI because of simple circuit configuration and low power consumption. Reducing the pattern geometry, e.g. the gate length and gate width, the operating range of the IC's will be expanded to G bit/s area.

Reference 1) H. Ishikawa et al."Normally-Off Type GaAs MESFET for Low Power, high Speed Logic Circuits," in 1977 IEEE Int. Solid-state Circuit Conf., Dig. Tech. Papers, pp.200-201.

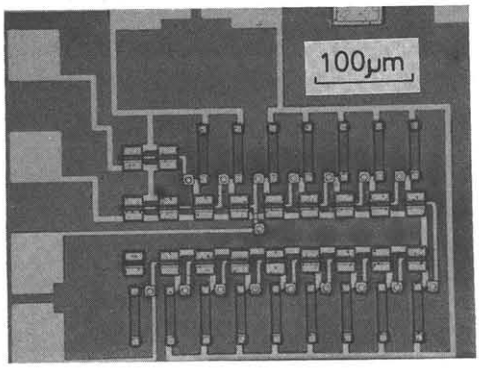

Fig. 1. Microphotograph of the test circuit consisting of a 13-stage inverter chain and an output buffer.

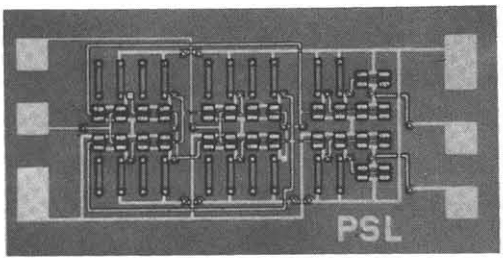

Fig. 3. Microphotograph of the binary frequency divider with a master-slave flip-flop.

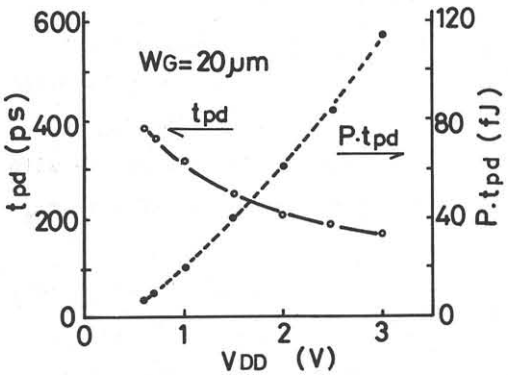

Fig. 2. Propagation delay time and power-speed product per gate as a function of the supply voltage.

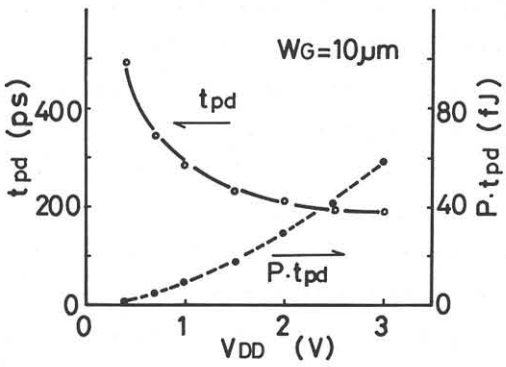

Fig. 4. Experimental results on the 13-stage ring oscillator with the 10-um wide gate FETs.