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C-1-1 Experimental Integration Technology for Josephson Tunneling Switching Devices

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INTRODUCTION Josephson tunneling switching devices are very attractive because of their high switching speed and low power dissipation. Success of such devices requires the development of fabrication technology which assures high production yield, uniform quality, high reliability, and high packing density. Integration technology for these devices was first proposed by Greiner.[1] In this paper, some improved modifications beyond Greiner's technology will be described and discussed.

MODIFICATIONS IN FABRICATION PROCEDURES A cross-sectional view of the Josephson switching devices to be fabricated is schematically shown in Fig. 1. One of the modifications is in the structure of a superconducting ground plane. An EB-evaporated high-quality Nb-film, instead of Greiner's rf-sputtered films, was deposited onto the Cr-overcoated Si-wafer substrate in the high vacuum below 10^{-5}Pa. Cr-overcoating was quite effective to achieve hard contact of EB-evaporated Nb-film to the substrate without degradation in superconducting property of Nb-film. A SiO_2 over-lying insulation layer was deposited by rf-sputtering. In this structure, the ground plane insulation upto a few μm in thickness is available with good thickness controllability.

Patterning of the ground plane was accomplished by chemical etching. During etching Nb-film, Cr-overcoated substrate was found to act as an excellent stopper against HF-HNO_3 etchant. Bonding lands of Au-Cr layered structure, which were quite resistive to mechanical stress during wire-bonding, were successfully formed on the SiO_2 insulation layer.

Second modification is in the oxidation technique for tunnel barrier formation. Our experimental oxidation chamber is shown in Fig. 2, where an additional ring-shaped rf-discharge electrode is provided behind the rf-sputter target. Wafers, on which sequentially-deposited 8%In-4%Au-88%Pb alloy electrodes and an Al-overcoated photoresist stencil for top electrode pattern[1] had been formed, were mounted on the target. Prior to oxidation, the base electrode surface was cleaned by rf-sputtering with Ar-discharge. Then, replacing Ar-gas by pure dry oxygen of about 1 Pa., weak rf-power was now supplied to the ring electrode and oxidation was carried out. Sequentially, Pb-Au alloy top electrodes were evaporated without breaking vacuum. In this technique, neutral oxygen radicals as well as non-accelerated oxygen ions are predominantly responsible for oxidation, while accelerated ions do so in Greiner's technique. Therefore, more reliable and uniform Josephson

devices without damage are expected.

Finally, SiO interlayer insulation and In-Au-Pb control lines were formed by means of Greiner's technology. A micrograph of the integrated Josephson switching device chip, thus fabricated, is shown in Fig. 3.

DEVICE CHARACTERISTICS Electrical characteristics of the fabricated switching devices were evaluated at 4.2°K. Figure 4 shows a typical switching threshold curve, or a maximum Josephson current vs control current curve, measured for a 60 μm long device. Josephson current density is roughly estimated as 500 A/cm^2, predicting Josephson penetration depth of 15 μm. The curve shown is in a good agreement with what is expected theoretically,[2] which demonstrates the device is spatially uniform. Spread of the device characteristics in the wafer was less than 25%. Also, no significant change in the characterisctics was observed after at least 10 repetitions of thermal cycling between 300°K to 4.2°K.

1) J. H. Greiner et al: J. Vac. Sci. Tech. 11(1974) 81
2) S. Basavaiah et al: IEEE Trans. MAG-11(1975) 759

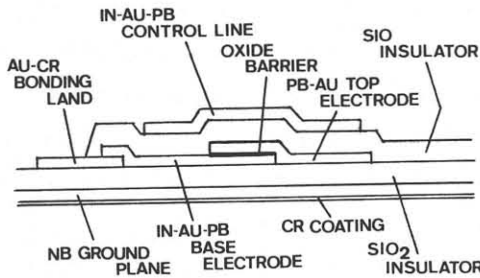

Fig. 1 Cross-sectional view of integrated Josephson switching devices.

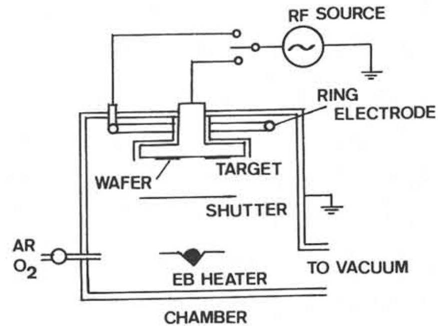

Fig. 2 Experimental oxidation chamber for tunnel barrier formation.

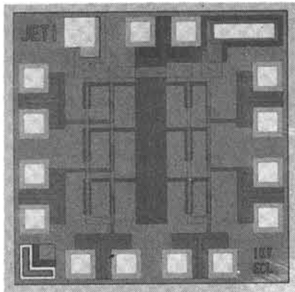

Fig. 3 Micrograph of the fabricated device array chip. A 3-mm square chip contains 6 switching devices of 30 μm-minimum width.

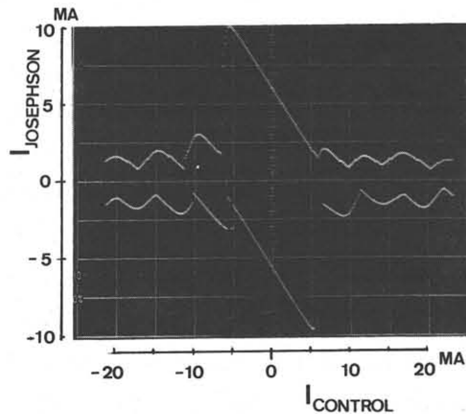

Fig. 4 Experimental switching threshold curve obtained in 30 x 60 μm device.