Digest of Tech. Papers The 11th Conf. (1979 International) on Solid State Devices, Tokyo

A — 0 — 1
(Invited)

Recent Progress and Potential of SIT

Jun-ichi Nishizawa

Research Institute of Electrical Communication, Tohoku University

Sendai 980, Japan

I. INTRODUCTION

As is well-known fundamental structure of the static induction transistor (SIT) is the short channel field effect transistor. Especially, the same series resistance r_s between the intrinsic gate point and the source electrode is reduced to decrease the effect of negative feed-back enough to fulfil the relation; $r_s \cdot G_m < 1$, where G_m is the intrinsic transfer conductance. As a result of the reduction of the source series resistance; r_s, the voltage-current character becomes to be non-saturating, mainly, Ohmic or exponential. The exponential character can be said as prepunch-through condition, in junction type or in insulated gated structure, which is followed by the punch-through condition; the current voltage characteristic follows space charge conduction law [1] as has been published in many papers [2].

This means that the SIT has always faster speed for operation, because of the smaller time-constant $r_s \cdot C_{GS}$, where C_{GS} is the gate-source capacitance.

The length between the intrinsic gate point and the drain is limitted by the transit time in high frequency devices, as same as the bipolar transistor (BJT) and the field effect transistor (FET). Collector or drain capacitance can be reduced contradicting to the determination by the influence of the transit time effect. Then the optimum thickness for the depletion layer is calculated to be the transit time equals to about 2 radians of the operating frequency [3].

If we drive the gate of SIT into forward voltage, the carriers overwhelming the barrier at the intrinsic gate toward the drain is increased similar to the BJT. SIT operating in this operation mode was named as bipolar mode SIT (BSIT), which has advantages not to have base resistance because the voltage at the intrinsic gate point is controlled through the capacitance and not to have storage effect because the potential distribution at the intrinsic gate point is like saddle which has no stable point for the storage of the injected carriers. Then BSIT has no storage capacitance but only depletion layer capacitance between the gate and the source and, moreover, there is no determination effect with the increase of the area, which makes possible to realize the high output power devices, even at higher frequencies.

Moreover, the noise generation in SIT is quite small which largely helps the lower power operation.

II. HIGH POWER -- HIGH FREQUENCY DEVICES

As has already been understood, SIT is much surperior to either BJT or FET as high frequency devices and, moreover, as high power devices. Because of the lack of the base resistance, as the high frequency device, the gain-boundwidth product in SIT can be given by (G_m/C) same as vacuum tube, where $C = C_{GS} + (k + 1)C_{GD}$, $k \fallingdotseq G_m/(C\omega_c)$, C_{GD} is the capacitance between gate and drain, G_m is the transfer conductance and k is the absolute value of the voltage gain. The estimated value of G_m/C_{GS} for U-MOS GaAs SIT is 1000 GHz.

As was mentaioned, this value is independent to the device area. This property is peculier to SIT; with the increase of the area, SIT does never deteriorate the high frequency character, however, increases the output power.

As the result, SIT is expected to very high power at very high frequency as shown in Fig. 1. Final limitation is expected to be the area of the semiconductor wafer.

III. SWITCHING DEVICES

In BSIT, very steep drain current increase with voltage has been observed. With the increase of gate or drain voltage less than 2 mV, drain current is increased more than 10^6 times [4]. This details will be given in another paper.

This phenomenon gives very good switching properties, switching time is less than 0.1 μsec for 20 A [5]. Same operation can be applied even for thyristor.

Even in the case of single mesh structure [6], switch off time in SIT thyristor is 2 μsec at 100 A [7]. Two mesh structure [6] is expected to show much faster speed, perhaps less than 1 μsec in the same current level.

And as is the same with in the case of SIT, properties of SIT thyristor is also expected to be independent on the area.

Normally-off, Normally-on and dc switching thyristor with pulse can be realized [8].

IV. LOW POWER DIGITAL APPLICATIONS

Now the Pτ product in real IIL equivalent junction type SIT integrated circuit shown less than 1 fJ till about 2 ~ 3 nsec operation [9], which is the limitation caused from the storage effect under the gate and has already expected much faster operation till about 10 psec in insulated gate structure [10].

Even in the simulation experiment using junction type SIT, current mode logic already shows the switching operation at about 1 nsec [11] and is expected the operation in the range of 100 psec in real junction type BSIT and less in U-MOS SIT.

Memory devices named as SIT memory has alrealy shown subnano second access time operation with the sustain time of 10 second which is expected to have a packing density of $10^7/cm^2$ [12], which is also expected to be applied for nondestructive read-out application combined with field effect devices as shown in Fig. 4 [13], and for image converter.

V. LINEAR A-D AND D-A INTEGRATED CIRCUIT

As is well known, SIT can be designed to have very linear character and is expected also to be very nice to realize linear, A-D and D-A integrated circuit.

VI. CONCLUSION

SIT is expected to be the most promising devices in very wide field high speed, high power, high packing density and low power operation integrated circuit.

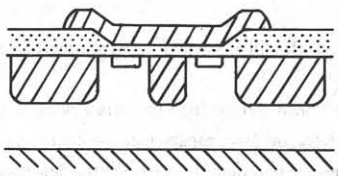

Fig. 5 Cross-sectional view of non-destructive read-out SIT memory.

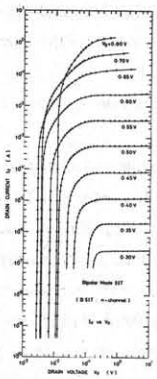

Fig. 2 Drain current vs. drain voltage in BSIT exhibiting very steep increase of drain current for the drain voltage.

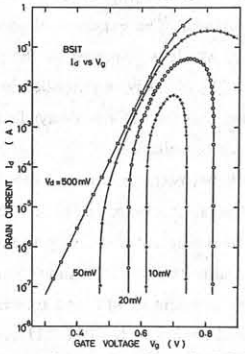

Fig. 3 Drain current vs. gate voltage in BSIT in low drain voltages, which includes very steep increase and drastic decrease of drain current.

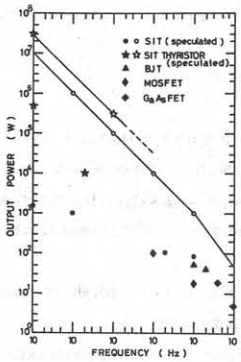

Fig. 1 Output power vs. frequency for BJT, FET, SIT and SIT thyristor including speculated values.

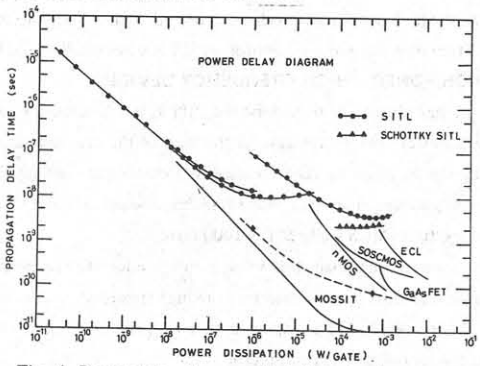

Fig. 4 Power-delay diagram of static induction transistor logic circuits including MOSSIT, where representative results of other logic circuits are also illustrated.

REFERENCES [1] Y. Watanabe, J. Nishizawa and Z. Yoshida, Busseiron Kenkyu, Vol. 41, p. 96 (Aug. 1951). Digest of Tech. Papers 3: 333 Joint Conf. IEEE, IECE and ILE of Japan (May 1951), W. Shockley and R.C. Prim, Phys. Rev., Vol. 90, p. 753 (1953). [2] P. Richman, IEEE Trans. on ED, Vol. ED-16, p. 759 (Sept. 1969), G.E. Neumark and E.S. Rittner, Solid State Electronics, Vol. 10, pp. 299-304 (1967), D. Frohman-Bentchkowsky and A.S. Grove, IEEE Trnas. on ED, Vol. ED-16, p. 108 (1969), V.G.K. Reddi and C.T. Sah, IEEE Trans. on ED. Vol. ED-12, p. 139 (1965). [3] J. Nishizawa and Y. Watanabe, Science Rep. RITU. B-(E-C), Vol. 10, No. 2, pp. 75-89 (1958). [4] J. Nishizawa, T. Ohmi, T. Matsuyama and Y. Mochida (in this conference). [5] J. Nishizawa, T. Ohmi, Y. Mochida, T. Matsuyama and S. Iida, Digest of Tech. Papers on 1978 IEDM, p. 676 (Dec. 1978). [6] J. Nishizawa, T. Terasaki and J. Shibata, IEEE Trans. on ED, Vol. ED-22, pp. 185-197 (April 1975). [7] Terasawa and Okamoto, to be published in this conference. [8] J. Nishizawa and K. Nakamura, Technical Digest of ESSDERC 78. [9] J. Nishizawa, T. Ohmi, Y. Mochida and T. Nonaka, IEEE Trans. on ED, to be published. [10] J. Nishizawa, Denshi Zairyo (Electronic Materials) Vol. 10, No. 9, p. 57 (Sept. 1971). [11] J. Nishizawa, N. Takeda and T. Ohmi, IEEE MTT Specialty Conf. on Gigabit Logic for Microwave Communications (Florida USA 1979). [12] J. Nishizawa, T. Tamamushi, Y. Mochida and T. Nonaka, IEEE Trans. on S.C., Vol. SC-13, p. 622 (Oct. 1978), J. Nishizawa, T. Tamamushi, T. Ohmi, T. Nonaka and Y. Mochida, to be published in IEEE Trans. on S.C. [13] J. Nishizawa, Japanese Patent App. No. 52-20653 (26th, Feb. 1977).