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A—1—6 Reactive Sputter Etching System with Floating Grid

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A planar-type reactive sputter etching (RSE) system with a floating grid was studied in an effort to eliminate damage induced into wafers during etching.

The RSE system has become an important technique for etching patterns of 1 μm or less on various materials required in fabricating very large scale integrated (VLSI) circuits.[1] Although the RSE system has the potential for satisfying the severe requirements for microfabrication of VLSIs, electrical damage induced into etched silicon wafers is an important problem in its application. When reactive gas molecules are discharged to form various reactive species, ions generated in the plasma are accelerated by the self-bias (SB) voltages which take place between two electrodes, which in turn strike the specimen surface and damage the wafer. Such damage was examined by analyzing MOS capacitors fabricated on etched Si wafers.[2] Figure 1 shows the surface state density (Nss) of an MOS capacitor as a function of SB voltage. The Nss related to the damage is greatly dependent on the SB voltage. To reduce SB voltage, a novel RSE system having a third electrode between the anode and cathode is proposed. The third electrode has many perforation, like the grid electrode in a vacuum triode, and floats between the other electrodes. By optimizing the configuration, the plasma density between the floating grid (FG) and cathode is increased compared with that of a conventional planar RSE system. Figure 2 shows the etch rates of (100) oriented Si as a function of the radio frequency (RF) input power. In the 50-1000 W RF power range, the etch rates for an RSE system with an FG are higher than those of a conventional RSE system. Figure 3 shows the SB voltages of an RSE system as a function of RF power. The SB voltages of an RSE system with an FG are 1/8-1/2 of those of an RSE system without an FG in this operation range. From these results, a practical etch rate ($\gtrsim$350A/min) with negligible side etching ($\lesssim$0.05μm) is obtained at an RF power above 100 W with a total gas pressure below 0.05 torr. Photo 1 shows an SEM photograph of etched polysilicon on silicon dioxide. The sample was etched at an RF power of 200 W with 0.01-torr CF_4 gas mixed with 5% O_2.

This study shows that a floating grid is useful in decreasing the self-bias voltage in an RSE system. Thus, an RSE system with an FG can be used as a novel, nondamaging etching technique to etch various materials used in MOS devices, especially single crystalline silicon substrates.

ACKNOWLEGMENTS

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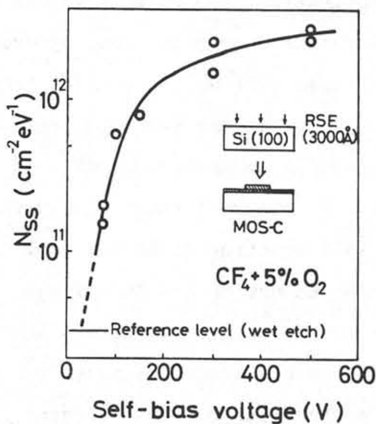

Fig. 1 Surface state density (Nss) vs. self-bias voltage (MOS capacitors are fabricated on a silicon surface after etching off a depth of 3000A.)

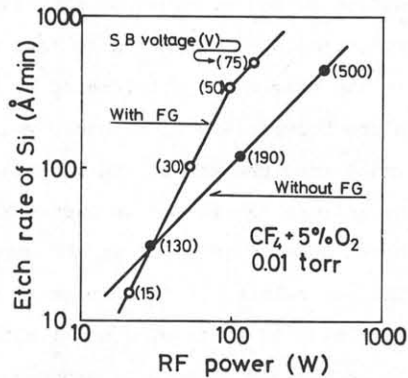

Fig. 2 Etch rates of Si vs. RF power (Values in parentheses are self-bias voltages.)

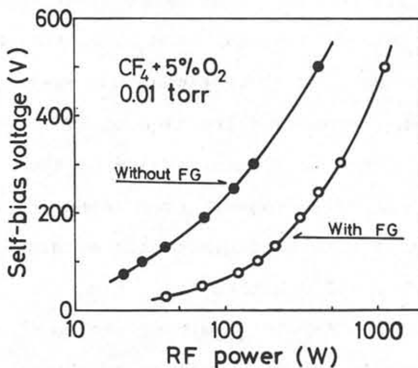

Fig. 3 Self-bias voltage vs. RF power

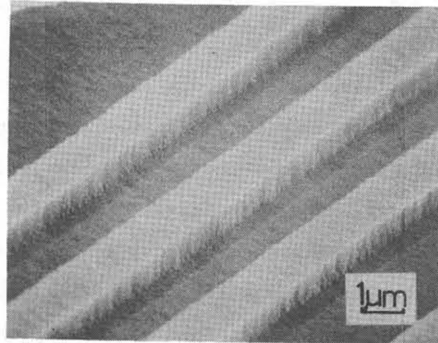

Photo 1 SEM photograph of 1μm line-width polysilicon removed a photoresist as etching mask