Digest of Tech. Papers The 11th Conf. (1979 International) on Solid State Devices, Tokyo

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Low-frequency Low-noise Transistors Fabricated by Double Ion Implantation

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Ion implantation has been used to fabricate base and emitter regions of silicon bipolar transistors. However, low-frequency noise performance of these devices has tended to degrade without optimizing the annealing process after ion implantation.[1] An attempt to improve noise performance has been carried out on implantation to poly-Si method for base formation.[2]

In this paper, two-stage annealing processes, i.e. low-temperature wet-oxygen oxidation and high-temperature dry-nitrogen drive in, for double-implanted trangistors are proposed to obtain improved device characteristics. The first low-temperature wet-oxygen oxidation process was considered to be effective to remove off the amorphous layers formed by ion implantation and surface contamination without inducing secondary defects. This surface removal might be considered as a possible cause of noise performance improvement. However, the impurity re-distribution after low-temperature wet-oxygen oxidation was found to be a serious problem especially in high dose P^+ implanted emitter regions. Present experiments show that a large amount of phosphorus atoms found to segregate in the growing SiO_2 films under certain conditions of implantation and oxidation, and h_{FE} controllability of the devices is discussed

The B^+ ions with a dose of $3\sim5\times10^{14}$ ions/cm^2 and P^+ ions with a dose of $1\sim3\times10^{16}$ ions/cm^2 were implanted at 30~40 keV for base and emitter regions, respectively. These implanted specimen were oxidized in a wet-oxygen ambient between 700°C and 1000°C. They were then annealed in a dry-nitrogen ambient at high temperature (typically 1200°C for base and 1100°C for emitter drive in). For comparison, conventional single-stage annealing in a dry-nitrogen at temperature above 1000°C was carried out.

Secondary defects after conventional dry-nitrogen annealing or two-stage annealing process were observed by TEM. Typical results are shown in Fig.1 for double-implanted (3×10^{14} B^+ ions/cm^2 and 3×10^{16} P^+ ions/cm^2 for base and emitter formation, respectively) specimens. Emitter edge dislocations were not observed in both specimens. Furthermore, surface contaminations which were considered to be SiC particles[3] disappeared in specimen put through the two-stage annealing process, although a large amount of SiC particles were detected in dry-nitrogen drive in specimen as shown in Fig.1. These results indicate that the low-temperature wet-oxygen oxidation process has the effect of cleaning implanted surface.

In B^+ implanted regions, good uniformity in sheet resistivity ($\sigma<1\%$) was performed with the oxidation for 60 min at a temperature below 800°C and high-temperature dry-nitrogen drive in process.

However with high dose P^+ implanted layers, a large number of phosphorus atoms were found to segregate in the growing SiO_2 films under certain implantation and oxidation conditions. Typical results of carrier concentration reduction are shown in Fig.2, along with the grown oxide thickness and ρ_s data for different oxidation temperatures. Carrier concentration and ρ_s for low-temperature wet-oxygen oxidized specimen were measured after annealing in dry-nitrogen for 40 min at 1100°C. Minimum carrier concentration was about 1/2 the implanted concentration for 3×10^{16} ions/cm^2 P^+ implanted layers at an oxidation temperature of 750°C. This carrier concentration variation corresponds to one order magnitude difference in mean value of h_{FE}, when the base formation process and emitter drive in process are fixed. Fine control and achievement of uniformity in h_{FE} should not be performed without considering this carrier reduction phenomenon. It was confirmed by electron probe micro-analysis (EPMA) measurement this total carrier concentration reduction correspond to the phosphorus atom inclusion into growing SiO_2 films. This phenomenon should be discussed taking into account of phosphorus diffusion and oxidation rate enhancement[4] in high dose P^+ implanted layers.

The two-stage annealing process was applied to base and emitter implanted low-frequency low-noise transistors with final emitter junction depths of typically around 2 μm. The equivalent noise voltage at 10 Hz as a function of h_{FE} is shown in Fig.3 for a number of the same structure devices fabricated with different processes. These curves show that the double-implanted devices have the best performance. Furthermore, the linearity of collector current dependence of h_{FE} (h_{FE} at 0.02 mA / h_{FE} at 2 mA) for the double-implanted devices improved to 0.9~0.95 comparing with conventional thermal diffusion transistors (around 0.75). Surface contamination reduction by wet-oxygen oxidation as mentioned above and the gettering effect of certain impurities might be considered as possible causes of improvement in noise performance.

Uniformity of h_{FE} of the double-implanted devices within ±5% around a wafer was obtained by optimizing the low-temperature wet-oxygen oxidation treatment and by achieving uniformity of implanted dose in a wafer with high current ion implantation machine.

The authors wish to express their thanks to Drs. I. Kanomata, N. Sakudo and K. Tokiguchi for helpful discussion and supporting of high current ion implantation experiment.

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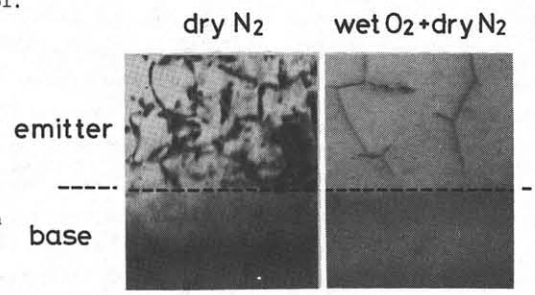

Fig.1 TEM micrographs of defects observed in the double-implanted specimens for dry N_2 annealing and two-stage annealing (wet O_2 and dry N_2).

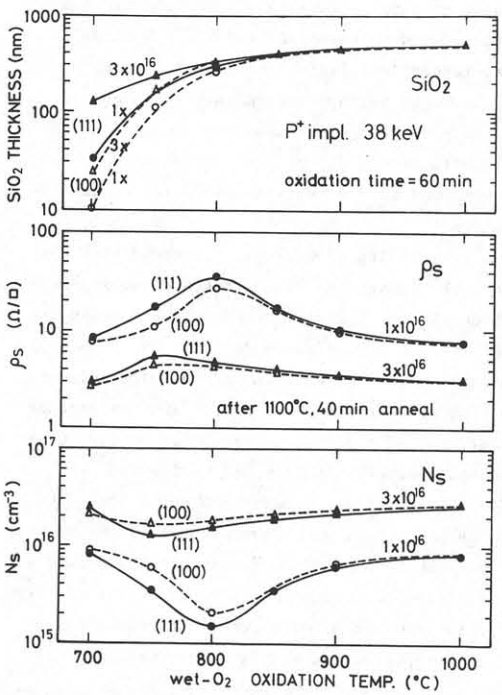

Fig.2 Variation of oxide thickness, sheet resistivity (ρ_S) and total carrier concentration (N_S) for 1 and $3x10^{16}$ ions/cm^2 P^+ implanted layers as a function of wet-oxygen oxidation temperatures (oxidation time = 60 min).

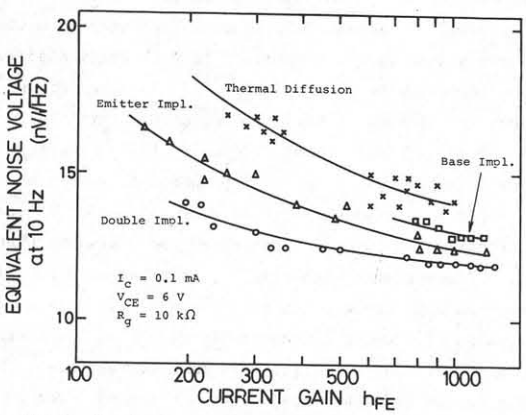

Fig.3 Equivalent noise voltage at 10 Hz vs. h_{FE} for a number of the same structure devices fabricated with different processes.