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Computer Aided Si-MOSFET Process Designing.

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The optimization of the fabrication processes is essential for LSI development. To attain this objective, it is desirable to combine the simulation of processing steps and that of the device characteristics.

A computer program which simulates each fabrication step and predicts the electrical characteristics of resultant MOS diodes and transistors has been developed. In this program, one-dimensional impurity distribution and oxide thickness are traced.

Fick's law with the moving boundary condition at $Si-SiO_2$ interface is utilized to predict the impurity distribution in oxidation and annealing steps. Impurity segregation effect is also considered. The Gaussian distribution and the range distribution theory in a multiple layer structure are adopted[1] for ion implantation step. The program also includes substrate definition, oxide etching and CVD steps.

One dimensional Poisson's equation with the Maxwell-Boltzmann charge distribution is solved for the obtained structure to estimate the device characteristics. Threshold voltage is defined as the gate voltage at which a certain number of mobile charges emerges in the MOS structure. Total and mobile charge distributions for MOS diodes can also be calculated at any given bias condition. One-dimensional charge distribution and the gradual channel approximation are combined to obtain I-V characteristics of MOS transistors.

Figures 1 through 4 show some comparison between theoretical predictions and experimental results. The device considered here is a Si-gate n-channel depletion load MOS transistor (W/L:200/200 μm). Process parameters are listed in Table 1. As can be seen, they are in good agreement, considering the various process fluctuations. This program can be used to estimate process sensitivities for various steps. An example is listed in Table 2.

In conclusion, an attempt has been made to predict MOS device's characteristics from process conditions. The resulted program was found to be a powerful tool for process optimization. The use of this program can reduce time consuming test runs.

Reference: 1)H.Ishiwara and S.Furukawa, Trans. Inst. Electronics Comm. Engrs, Japan Pt.C Vol. 56 C, p179 (1973)

Table 1 Input process data.

1. SUBSTRATE	B=2.5E15 (511)	
2. OXIDATION(Gate)	TEMP=950. TIME=76. DRY	
3. IMPLA	B=5.5E11	ENERGY=40.
4. IMPLA (A)	AS=1.6E12	ENERGY=150.
(B)	AS=1.2E12	ENERGY=150.
(C)	AS=8.4E11	ENERGY=150.
5. ANNEAL	TEMP=900.	TIME=35.
6. ANNEAL	TEMP=950.	TIME=30.
7. ANNEAL	TEMP=1000.	TIME=20.

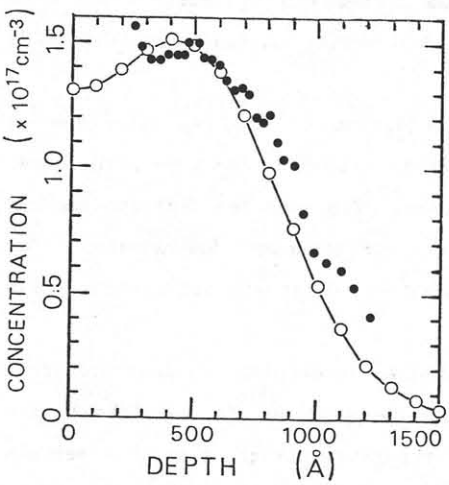

Figure 1 Arsenic distribution after processing; calculated (o), and measured (•) by C-V method.

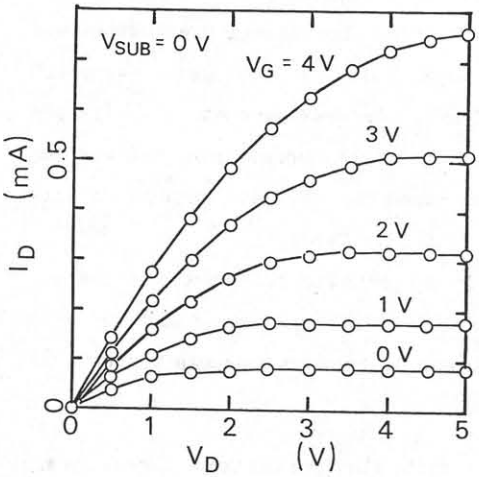

Figure 2 Calculated drain current of the transistor (process A).

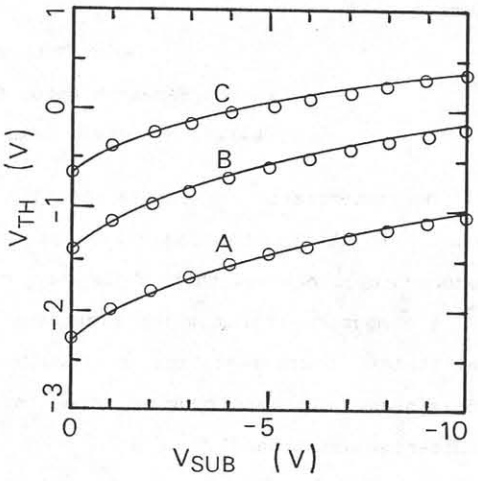

Figure 3 Threshold voltage as a function of substrate bias; calculated (o), and measured (-).

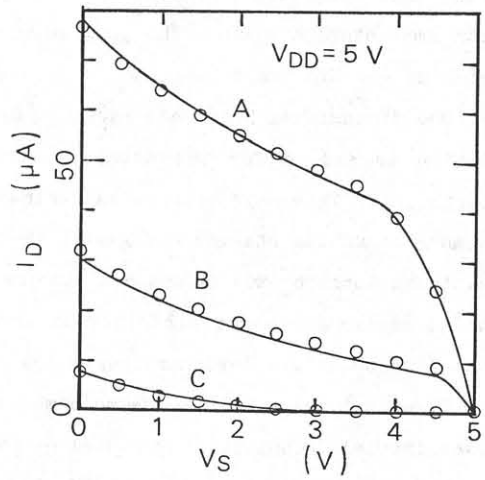

Figure 4 Calculated (o), and measured (-) load lines.

Table 2 Process sensitivities for load current of the transistor (process A) at V_{DD} = 5 V, V_S = 0 V and V_G = V_S. Normal current is 76 μA.

Substrate impurity density		-0.24	%/%
Gate oxidation	/Temperature	-0.50	%/deg
	/Duration	-0.43	%/min
As^+ implantation	/Energy	0.94	%/KeV
	/Dosage	2.9	%/%
1000°C annealing	/Temperature	0.020	%/deg
	/Duration	0.45	%/min