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Short Channel MOS FET's Fabricated by Self-Aligned Ion Implantation and Laser Annealing

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Laser annealing of ion implanted layers has recently been recognized as a possible substitute for conventional furnace annealing in device fabrication[1,2]. With this technique, heating can be limited to the surface layer, and the substrate surface under proper mask materials is not heated. These features are extremely useful for fabricating short channel MOS FET's, since shallow source and drain, which are essential to realize short channel devices, can be made easily. Furthermore, such structures can be made by the combination of self-aligned ion implantation and laser annealing, both to the gate electrode. Under such background, this paper describes the depth and lateral diffusion of ion implanted atoms by laser annealing and the characteristics of short channel MOS FET's.

First, carrier concentration profiles of P^+ (50 keV, 8×10^{15} cm^{-2}) and As^+ (80 or 150 keV, 8×10^{15} cm^{-2}) implanted layers after Ruby laser annealing (duration time; 25 ns, energy density; $\sim$1.4 J/cm^2) and furnace annealing (800—1100 °C, 30 min) are precisely compared. The result shown in Fig.1 indicated that carrier concentration profiles after laser irradiation were narrower than those resulting from furnace annealing, though they spread as laser energy increased. Furthermore, peak carrier concentrations were higher by a factor of three. In laser annealing, as surface regions of the substrates were raised to high temperatures and melted, all implanted atoms were incorporated into the substitutional lattice sites[3]. Substitutional atoms were then quenched to a metastable state very rapidly (10^{10} deg/s), thus excess solubility of impurity atoms is realized. Furthermore, short annealing time (0.1 μs) keeps impurity atom from diffusing into deeper regions. Sheet resistivities and junction depths after laser annealing are compared with results obtained by conventional furnace annealing in Fig.2. The results clearly demonstrate that shallow junction depths with low resistivities were only realized by laser annealing.

Lateral diffusion of implanted atoms as a result of laser annealing was examined by SEM. Samples were prepared by As^+ implantation and followed by laser irradiation through a partial mask of poly-Si films (3500 Å). The cross section of the laser irradiated region was compared with that of furnace annealing in Fig.3. Lateral spread of As atoms from the mask edge was very small, thus implanted regions are self-align annealed to the mask edge by laser irradiation.

On the basis of above results, short channel MOS FET's were fabricated. Source and drain regions were formed by As^+ ions (80 keV, 1×10^{16} cm^{-2}) implanted through 300 Å oxide film after formation of gate oxide (500 Å) and phosphorus doped poly-Si gate electrodes (3500 Å). A Ruby laser (0.4 - 1.4 J/cm^2) was then irradiated onto the samples to anneal implanted source and drain regions. Samples were then annealed (415 °C, 30 min) in hydrogen ambient after formation of Al electrodes. The p-n junction characteristics depended very much on the laser irradiation energy. Optimum laser energy density was 0.79 J/cm^2 during these prosesses. Reverse current levels of 2×10^{-9} and 2×10^{-8} A/cm^2 at 0.01 and 1 V were comparable to those of diodes fabricated by conventional furnace annealing.

Lateral junction characteristics at the edge of implanted regions under gate electrodes were examined by measuring the drain current—gate voltage characteristics in the subthreshold region. They were found to be the same as those of furnace annealed samples with a semilogarithmic slope, α, of 80-90 mV/decade. This fact indicates that the edge of implanted and annealed region under the gate electrode has no defective structure that affects electrical characteristics[4].

Drain current-voltage chracteristics of MOS FET's with channel length (L) of 1.5 and 2.5 μm are shown in Fig.4. The threshold voltage (V_{tn}) vs channel length relations are shown in Fig.5

and compared with those of high temperature thermally annealed conventional devices. The curve for the laser annealed samples is seen to shift toward the short channel region. Overlapping capacitance between gate and source or drain were reduced to about 50 % that of furnace annealed samples. These improvements are the result of small lateral and depth diffusion of implanted As atoms.

In conclusion, formation of shallow junction with low resistivities and self-aligned annealing to gate electrodes were established utilizing laser annealing. These features were effectively applied to short channel MOS FET's.

References

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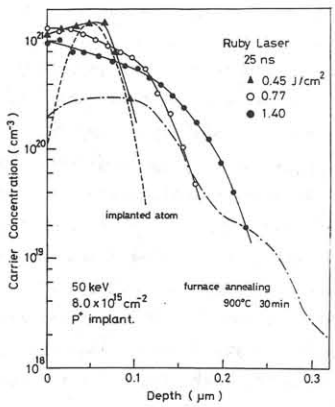


Fig.1 Carrier Concentration Profiles

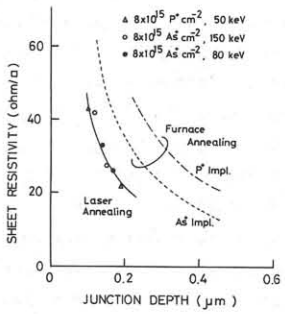


Fig.2 Relation between Sheet Resistivities and Junction Depths

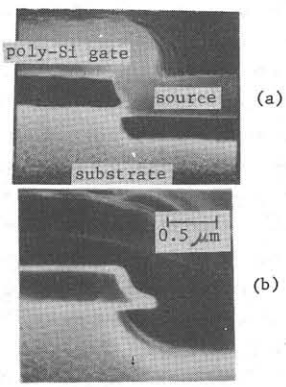
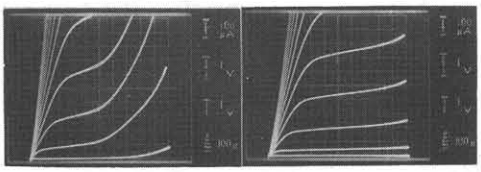


Fig.3 Cross-Section of Annealed Region
(a) Laser Annealing
(b) Furnace Annealing



L = 1.5 μm L = 2.5 μm

Fig.4 MOS Characteristics

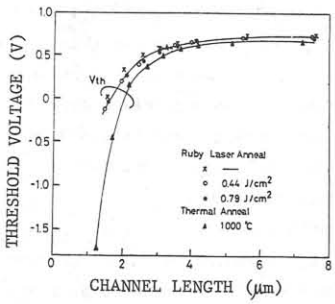


Fig.5 Relation between V_{th} and L