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Is SOS ready for VLSI ?

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From the beginning Silicon on Sapphire (SOS) technology has been considered as an ideal MOS technology because of the very small amount of parasitic capacitances associated with a thin layer of silicon on an insulating substrate. This is particularly true for high speed operation and/or for low power consumption when CMOS technologies are considered (dynamic power consumption is involved). Main difficulties, when using this technology, have been found in high leakage currents (a past history !) and in higher substrate costs (a still existing situation) when compared to CMOS on bulk. Air isolation of devices provides both the capability of high speed operation and of narrowing gaps between adjacant devices, a very attractive property for high density technologies.

As far as VLSI is concerned, this means in a first step 2 µm channel length MOSFETS with thin SiO_2 layers (30 to 50 nm). The scaling rules are well known for bulk devices but seem less obvious for SOS devices mainly because leakage currents behavior versus channel length. Present results indicate that leakage currents below 10 pA/µm are achievable even with 2 µm channel length provided that "cold" processes are used, even for devices operated in the deep depletion mode. One basic advantage of SOS is that one more parameter is available in scaling down devices, the silicon epilayer thickness. This gives a possibility of avoiding punch through (thin epilayers) without increasing substrate doping.

The optimum situation will be reached for a silicon thickness such that minimum doping level in the layer can be used (intrinsic layer) for lower impurities scattering without facing too low mobilities when approaching the silicon-sapphire interface (higher crystal defects density). This is the optimum range of operation for the silicon on sapphire technology at a given state of the art of material quality.

Based on the above considerations thin silicon epitaxial layers (down to 80 nm) have been used showing good device characteristics and specific ability for VLSI (at reasonable source and drain sheet resistances).
The process is naturally planox and with a figure of merit well below 0,1 pJ (0,2 mW x 0,5 nsec) sub nanosecond logic circuits are feasible at very low power consumption challenging ECL circuits speeds (with two order of magnitude less power consumption).

Finally material extra cost is no longer and economic limitation for VLSI if higher density circuits are compared to the bulk parts (higher yields and more candidates per chip).

Presently it appears that CMOS/SOS and VLSI are becoming engaged before they get married to give birth to a SUPER CMOS technology.