

High Speed C-MOS IC Using Buried SiO₂ Layer Formed by Ion ImplantationKatsutoshi Izumi^{*}, Masanobu Doken and Hisashi Ariyoshi^{**}Research and Development Bureau^{*}, and Musashino Electrical Communication Laboratory^{**}
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MOS devices similar to SOS structure were fabricated utilizing a buried SiO₂ layer formed by oxygen ion implantation into silicon for the purpose of device isolation (this technology will be referred to as SIMOX, the abbreviation of Separation by Implanted Oxygen).

A transition layer, which is the silicon region above the buried SiO₂ layer, is required to grow epitaxial silicon layer. Based on consideration of the transition layer and the values from the table¹⁾, given by B.J.Smith, oxygen ions were implanted into silicon substrate under conditions of an implantation energy of 150 KeV and a dose of 1.2×10^{18} ions/cm². Electron diffraction pattern of the transition layer showed the fine Kikuchi lines in the diffraction pattern after annealing at 1150 °C for 2 hours.

Infrared spectra of implanted SiO₂ layer showed the well known absorption peaks for thermally grown SiO₂ after annealing above 900 °C for 1 hour. The other properties of implanted SiO₂ layers had become equivalent to that of the thermally grown ones by post-implantation annealing.

Field effect mobilities of holes and electrons in epitaxially grown silicon were 240 and 610 cm²/Vs for 5 V gate bias respectively. These values are equivalent to those of the bulk type devices. These are shown in Fig.1.

Gated p⁺-n junction diodes were fabricated in the silicon islands which were completely surrounded by the buried and thermally-grown SiO₂ layers. A typical diode whose ratio of W/L was 40 μm/40 μm exhibited excellent leakage-current characteristics as shown in Fig.2. The current was only 1×10^{-12} A for 10V reversed applied voltage at 0 V gate bias.

Figure 3 shows a cross-sectional view of MOSFET/SIMOX fabricated in this work. The thickness of the gate oxide and the height of the silicon island were 700 Å and 0.5 μm, respectively. The operational properties of 21-stage CMOS/SIMOX ring oscillator having 3.1 μm effective channel length are exhibited in Fig. 4. The propagation delay time and the dissipation power were 0.83 ns/stage and 0.33 mW/stage respectively, for 5 V operation of the oscillator.

This high speed operation can be attributed to the good monocrystalline state of the epitaxially-grown silicon layers and to the reduction of the parasitic capacitance by the buried SiO₂ layer.

One of the interest features of SIMOX is that the short channel effect of the CMOS fabricated in this work was not observed as far as the effective channel length comes to $1.8\mu\text{m}$, as shown in Fig. 5.

Reference

- 1) G. Deary, et al. : Ion Implantation, 1973, North-Holland Pub.

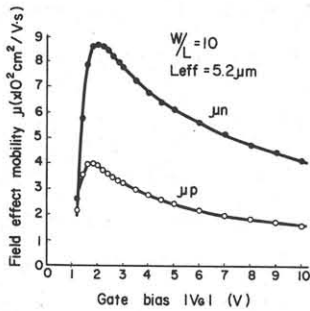


Fig. 1 Dependence of field effect mobility on gate bias.

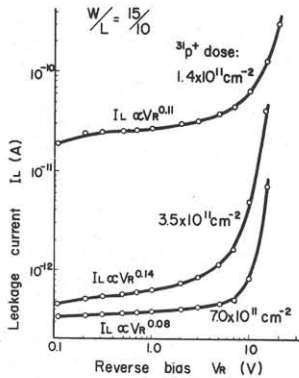


Fig. 2(b) Reverse characteristics of gated p⁺-n junction diodes.

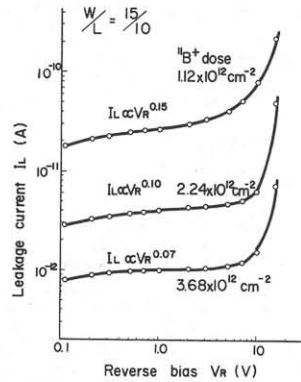


Fig. 2(a) Reverse characteristics of gated n⁺-p junction diodes.

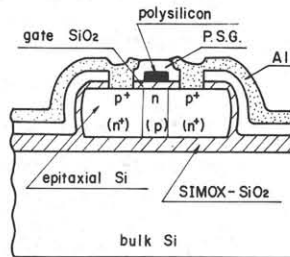


Fig. 3 Cross-sectional view of MOS FET / SIMOX

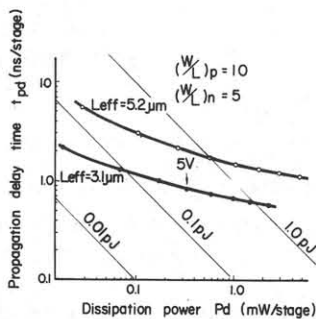


Fig. 4 Propagation delay time of the 21-stage CMOS/SIMOX ring oscillator as a function of dissipation power.

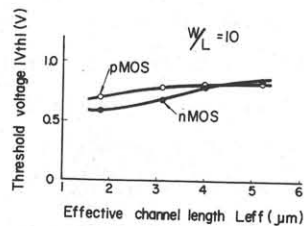


Fig. 5 Dependence of threshold voltages for both pMOS and nMOS FETs on the effective channel length.