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A — 3 — 8 Charge Pumping Memory with SOS-MOS Transistors

N.Sasaki, M.Nakano and T.Iwai

IC Division, Fujitsu Limited, Kawasaki 211, Japan

It has been presented that an SOS-MOS transistor can be a dynamic RAM cell by itself without any additional storage capacitor.[1] The new memory cell is called the "Charge Pumping memory" (CP-memory) cell. In this paper, the CP-memory is described as a memory array and the selective READ/WRITE operations are validated. The CP-memory is suitable for a large scale high density RAM because it has such advantages as non-destructive readout and non capacitance-ratio problem as well as the simple cell structure.

The information of the CP-memory cell is stored in the floating substrate of an SOS-MOS transistor as a potential difference. READ is carried out by measuring the threshold voltage change (the substrate bias effect). WRITE '1' is performed by charge pumping; the channel carriers are injected into the substrate and recombine there, resulting in the reverse-biased junctions at the source and drain. WRITE '0' is performed by the avalanche multiplication at a junction; the majority carriers are injected into the substrate.

The CP-memory test structures were made in a conventional p-channel self-aligned silicon gate process, using the (100) 1.0 μm thick non-doped silicon epitaxial film on sapphire. The film was doped n-type by phosphorus ion implantation at 180 keV to $4 \times 10^{12} cm^{-2}$ through the gate oxide. The gate oxide thickness was 700 Å. The threshold voltage was 4 V.

A memory array of the CP-memory is shown in Fig.1. The selective operations were proved using a test CP-memory; both the channel length and width are 40 μm. The voltages for the operations are summarized in Table I. For storage, the bit lines are kept at the power supply voltage V_{CC} and the word lines at zero volt. Information in a particular memory cell MC_1 is read when the selected bit line B_1 is set at zero volt and the word line W_1 is set at a readout voltage V_R, where V_R is larger than the threshold voltage and low enough to avoid charge pumping. The output voltage V_{OUT} corresponding to the drain current of the CP-memory cell was obtained as 6 mV or 18 mV, depending upon whether '1' or '0' is written. To write '1' in the cell MC_1, the bit line B_1 is set at zero volt and a charge pumping pulse V_{CP} is applied to the word line W_1. Charge pumping at the cell MC_3 is excluded by keeping B_2 at V_{CC}. Figure 2(a) shows that '1' is written in MC_1 by the pulse V_{CP} and the '1' is measured by the pulse V_R. Whereas the '0' in MC_3 is not affected by the pulse V_{CP}, since B_2 is kept at V_{CC}, as shown in Fig.2(b).

To write '0' in MC_1, every word line except W_1 is set at V_{CC} and an avalanche multiplication pulse V_{AVA} is applied to B_1. The pulse height V_{AVA} is adjusted to a proper value to exclude the multiplication at the cell MC_2 whose gate voltage is aet at V_{CC}. Figure 3(a) shows that '1' written in MC_1 is changed to '0' by the pulse V_{AVA}. Whereas the '1' in MC_2 is not altered by V_{AVA} because W_2 is set at V_{CC}, as shown in Fig.3(b). It should be noted that the non-destructive readouts of '1' and '0' are shown in Figs. 2(a) and 3(a), respectively.

The similar results were also obtained for the CP-memory test array shown in Fig.4; the channel length was 8 μm and width 10 μm.

Reference

1) N.Sasaki et al. : 1978 IEDM Tech. Dig. (1978) 356.

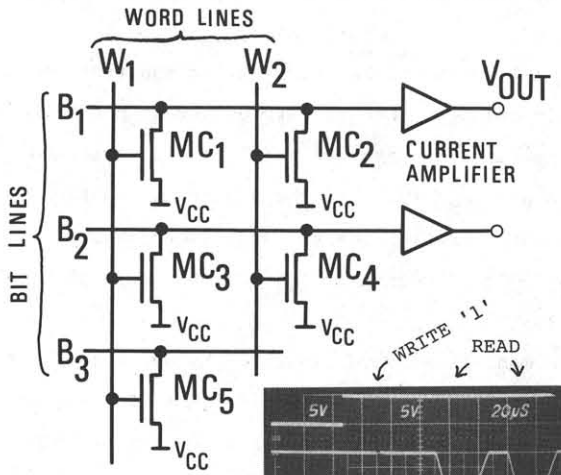
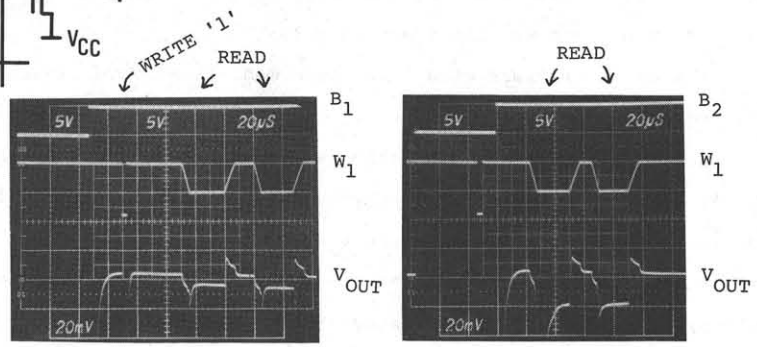


Fig.1 CP-memory array.

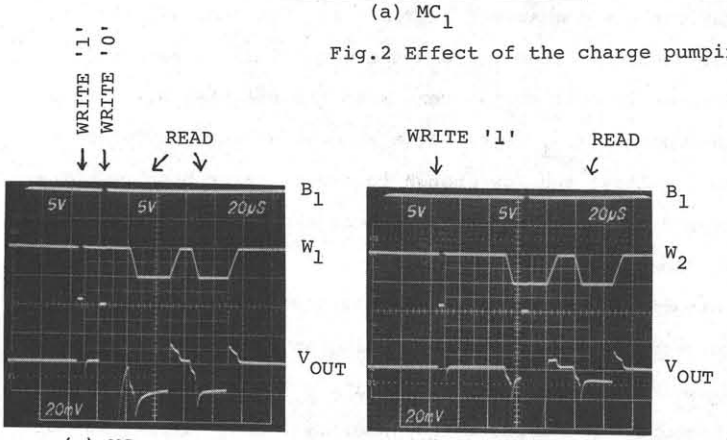
Table I. Voltage for the memory operations.

V_{CC}	-5 V
V_R	-5 V
V_{CP}	-9 V
V_{AVA}	-20 V



(a) MC_1 (b) MC_3

Fig.2 Effect of the charge pumping pulse.



(a) MC_1 (b) MC_2

Fig.3 Effect of the avalanche multiplication pulse.

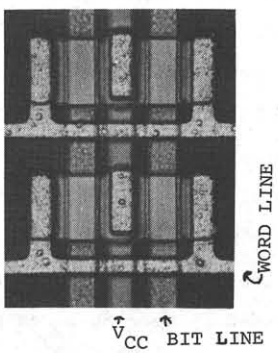


Fig.4 Photomicrograph of the CP-memory array.