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Electron-Hole Pair Generation at the Silicon-Sapphire Interface of SOS Devices

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Ultra-high speed silicon MOS circuits will require the use of epitaxial silicon on sapphire to reduce parasitic capacitances inherent in p-n junction isolation of bulk silicon circuits. The silicon/sapphire interface is recognized as the locus of intense electron-hole pair generation which contributes to leakage currents, and is suspected of being responsible for certain discrepancies[1] between observed transistor behavior and that expected from existing transistor models.

We shall describe electrical measurements performed on an epitaxial n^--silicon on sapphire test structure which can be used as MOS capacitor, n-channel depletion mode or p-channel enhancement mode transistor, and gated p-n diode. The measurements include MOS C-V characteristics, MOSC transient current after a gate voltage change, p-enhancement and depletion mode transistor conductances, and gated p-n junction diode I-V characteristics. The transient MOSC current and the steady state gated diode I-V characteristics will be shown to be correlated, so that one can be derived from the other. The experimental data indicate that electron-hole pair generation for fully depleted silicon does not occur uniformly along the silicon-sapphire interface, but is instead substantially restricted to the portion of the interface located under the rim of the gate electrode to which the depleting bias voltage is applied. This phenomenon results from electron accumulation at the sapphire interface under the gate interior necessitated by the lateral diffusion-controlled outflow of the generated electrons.

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1. "Frequency Dependent Propagation Delay in Silicon-on-Sapphire Digital Integrated Circuits", S. Sheffield Eaton and B. Lalevic, Solid State Electron. 21, 1253-1257 (1978).