Digest of Tech. Papers The 11th Conf. (1979 International) on Solid State Devices, Tokyo

A—4—1 Yield Modeling of Bipolar Integrated Circuits

D. Kranzer and H. Murrmann
Siemens AG, Integrated Circuit Division
Balanstraße 73, D-8000 Munich 80, FRG

Yield is very important for the fabrication of integrated circuits because of its drastic and direct effect on costs. An integrated circuit may fail at the wafer test because of a systematic failure (design error, violation of design rules etc.) or because of random local defects (pinholes, crystal defects etc.). Systematic failures should be eliminated during the development phase of an integrated circuit while the generation of random local defects are practically not avoidable.

In this contribution we will discuss the effect of random local defects on the yield of modern bipolar integrated circuits. The yield equation /1/ is reanalysed in the first part. Based on the generalized yield equation

$$Y = \prod_{i}^{n} (1 + \bar{D}_i s_i^2 F_i)^{-\frac{1}{s_i^2}} \qquad (1)$$

the yield modeling procedure is discussed.

In equation (1) the symbols have the following meaning:

- F_i is the spezific area susceptible to the defect type i under consideration,
- $\bar{D}_i$ is the mean defect density, and
- s_i is a statistical parameter characterizing the defect distribution; s_i is given by

$$s_i = \frac{\sqrt{\text{var } D_i}}{\bar{D}_i} \qquad (2)$$

  and
- n is the number of the relevant defect types.

Equation (1) contains a set of parameters $\{F_i\}$ determined by the layout and the remaining parameters $\{D_i, s_i, n\}$ depend on the process and its maturity. The process dependent parameters can be obtained by means of adequate test structures. For a given layout, the yield of an integrated circuit can be predicted with the aid of equation (1). Furthermore, the yield analysis reveals the dominating kind of defect. For a certain set of $\{\bar{D}_i, s_i, n\}$ this type may vary depending on the layout related parameter set $\{F_i\}$.

In the second part we discuss the test structures and the results obtained. It turns out, that the statistical parameters s_i's are approximately constant for a distinct defect type while the $\bar{D}_i$'s may vary from sample to sample considerably. A 128bit /2/- and a 1024x4bit ECL-RAM /3/ serve as examples to illustrate the application of (1). The yield has been constantly monitored by measuring the parameter set $\{\bar{D}_i, s_i, n\}$ on test patterns inserted on actual production wafers. Using (1) the calculated yield is usually in good agreement with the actual measured yield including correlations to the test hierarchy with tests of increasing complexity.

References

/1/ H. Murrmann and D. Kranzer, Siemens Entwicklungs- und Forschungsberichte (in press)

/2/ U. Bürker and P. Rydval, Siemens-Zeitschrift 49 (1975) 160

/3/ U. Bürker and H. Glock, ISSC, Philadelphiia 1979, 102