A — 4 — 3 A New Transistor Structure for High Speed Bipolar LSI

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A high speed bipolar transistor structure using a new isolation and polycrystalline silicon electrode technology has been developed especially with respect to minimum base and collector geometry. The new structure can minimize base and collector resistance and also storage capacitance, which result in high cut-off frequency f_T.

The process which fabricates the new structure is as follows. After a thick oxide layer is thermally grown to the thickness of 1 μm on a p-type starting wafer, windows of buried layer are opened by standard photolithography procedures. The buried layer is formed with heavy dose arsenic implantation and subsequent thermal annealing to a depth of about 4 μm(Fig. 1-a). Without removing the thermally grown oxide, n-epitaxial layer of 1.8 μm and polycrystalline silicon are grown simultaneously on the buried layer and on the thick oxide, respectively(Fig. 1-b). After that, unnecessary polycrystalline silicon is selectively removed by means of dry etching. The new transistor structure is made both in the remaining poly- and single crystalline area(Fig. 1-c). The next step is to make a base electrode with deep and heavy boron implantation(50 keV, 2×10^{15} cm^{-2}) into polycrystalline silicon. The intrinsic base is also implanted with boron to the dose of 7×10^{13} cm^{-2}. Then, the wafer is coated with CVD SiO_2 and annealed in N_2 ambient. The intrinsic base depth is about 0.5 μm and the boron implanted into polycrystalline silicon reaches the thick oxide surface, and this can lower base resistance(Fig. 1-d). After all contact windows are opened, the base contact windows are covered with oversize photoresist masks , then emitter and collector are implanted with arsenic(Fig. 1-e)[1]. Removing the photoresist masks, the emitter is annealed in N_2 ambient(Fig. 1-f). Then, the wafer is subjected to metallization.

Figure 2 shows the scanning electron microscope(SEM) photograph corresponding to the fabrication step (b) in Fig. 1. Figure 3 also shows the SEM photograph of the top view of this structure before metallization. Figure 4 shows the I-V characteristics of this new transistor, of which emitter size is 3x4 μm^2. The typical value of current gain h_{FE} was 30, BV_{CBO}; 12V, BV_{CEO}; 12.5V, BV_{EBO}; 5.4V and C_{TC}; 0.09 pF. The maximum f_T measured with S-parameter test set was 1.5 GHz.

Inherent high performance of this device will be expected in the LSI applica-

tion. Figure 5 shows a cross section of this new device (a) in the LSI, compared with that of a conventional oxide isolated transistor (b). In this figure, (1) an active area is reduced to one half or one third; (2) polycrystalline silicon are utilized both as internal wiring and resistors with minimum storage capacitance; (3) as a result, parasitic capacitance can be minimized.

In summary, high performance transistor has been developed by using a new isolation and polycrystalline silicon electrode technology. The improved points of this structure are as follows.

1. The small C_{TC} and C_{TS} are obtained due to the reduction of the inactive area and separation of the inactive area from the active area.
2. Internal wiring can be easily done by utilizing polycrystalline silicon.
3. Base and collector series-resistance can be lowered.

The new structure is expected to realize high performance and high complexity LSI.

(1) Y. Akasaka et al., 1978 IEDM 8-4 p.189 (Washington, 1978)

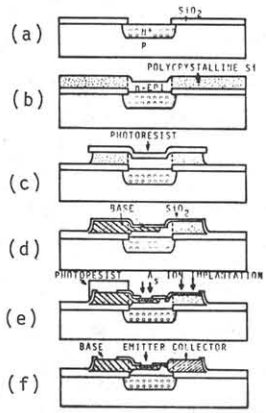

Fig. 1. Fabrication steps of new transistor structure

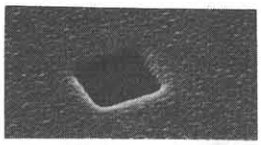

Fig. 2. SEM photograph of top view structure corresponding to the fabrication step (b) in Fig. 1.

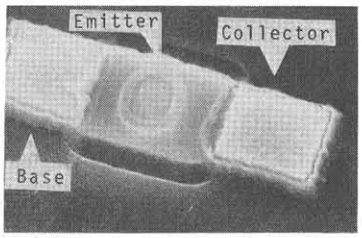

Fig. 3. SEM photograph of top view of new structure corresponding to the fabrication step (f) in Fig. 1.

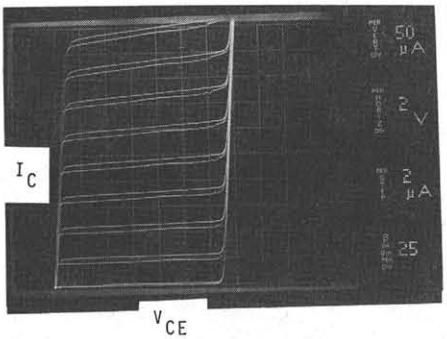

Fig. 4. I-V characteristic of a new transistor.

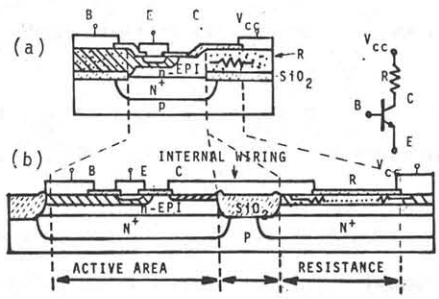

Fig. 5. Comparison of new structure (a) and conventional oxide isolated device (b).