A—4—4 A single-chip speech synthesizer for the PARCOR CODEC

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A high speed 16 bit digital signal processor with a multiplier, using 2 μm E/D n-MOS microfabrication technology, has been developed. A single-chip speech synthesizer for the PARCOR CODEC is realized by utilizing the signal processor. A high speed operation of 200 ns instruction cycle time and a low power dissipation of 450 mW have been achieved.

PARCOR is a voice-band compression technology that codes and decodes speech signals using PARtial autoCORrelation coeffiecients[1]. The PARCOR synthesizer can generate high quality human speech from data of less than 2,400 bits per second. Human speech is synthesized by processing sound source parameters in a multistage lattice filter based on a vocal-tract model. Figure 1 shows one stage filtering operation of the lattice filter used in the PARCOR synthesizer. The speech synthesizer consists of a controller, and the lattice filter which includes one multiplier, one adder/subtracter, one shifter, and registers as delay elements. A functional block diagram of the speech synthesizer is shown in Fig. 2.

The synthesis operation is triggered by an external start signal and is fully controlled by a sequence program stored in the ROM on the chip. The synthesized speech signal is obtained every 125 μs in the form of a PCM signal by repeating the filtering operation as shown in Fig. 1. One synthesis cycle consists of 160 instruction cycles, of which one cycle corresponds to a system clock rate. The data format of the input signals of the synthesizer is 16 bit fixed point 2's complement. The number of filter stages can be altered to either 8 or 10 by an external signal, according to the demanded quality. Moreover, a high quality of synthesized speech is attained by rounding off the multiplied results to 16 bits and replacing the value of the overflowed results with ± 1.

The 16 x 10 bit parallel multiplier achieves a high speed operation of 125 ns in simulation and an integration density of 2,300 transistors/mm^2, using a modified Booth's algorithm and cellular array formation. A carry look-ahead technique for high speed operation is adopted in the parallel 16 bit adder/subtracter. A static 22 word x 16 bit RAM is used as a register file. The controller consists of a 2,240 bit ROM which stores a sequence program, an 8 bit program counter, and other logic gates.

Figure 3 shows a photograph of the PARCOR synthesizer chip 3.65 mm x 3.7 mm in size. The chip contains 11,500 transistors (approximately 3,500 gates). The

process technologies, including 2 μm ultraviolet photolithography and 500 Å gate oxidation, are shown in Table 1. The threshold voltages of the transistors used are 0.8 V and -2.6 V. The measured maximum system clock rate and power dissipation are 5 MHz and 450 mW, respectively. The output wave form of the synthesizer is shown in Fig. 4. The power supply voltage is a single 5 V. The I/O interface is fully TTL compatible. Typical characteristics of the synthesizer are summarized in Table 2.

Reference

1) F.Itakura, et al., IEEE Trans. Communications, vol. COM-20, pp.792, Aug. 1972.

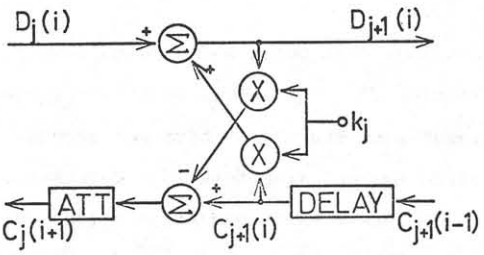

Fig. 1 One Stage Filtering Operation of the Lattice Filter

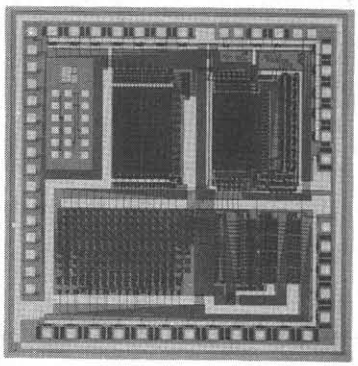

Fig. 3 Synthesizer Chip Photograph

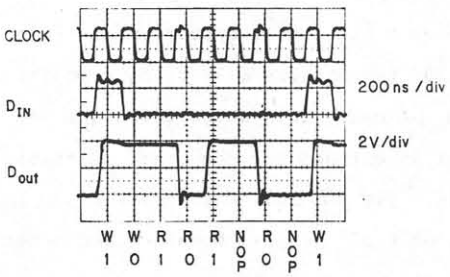

Fig. 4 Output Waveform

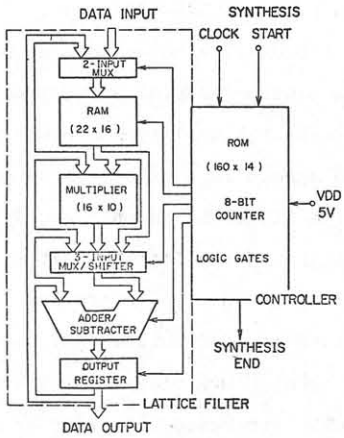

Fig. 2 Synthesizer Block Diagram

Minimum Line Width	2 μm
Minimum Pitch of Line and Space	6 μm
Gate Oxide Thickness	500 Å
Junction Depth	0.25 μm
Transistor Channel Length	2 μm
Minimum Channel Width	2.5 μm

Table 1 Process Technology

Technology	n-Channel E/D MOS
Chip Size	3.65 mm x 3.7 mm
Number of Gates	3,500
Number of Elements	11,500
Power Supply	5 V Single
Maximum System Clock Rate	5 MHz
Power Dissipation	450 mW

Table 2 Characteristics of Synthesizer