Digest of Tech. Papers The 11th Conf. (1979 International) on Solid State Devices, Tokyo

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ADAPTIVE WAFER SCALE INTEGRATION

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Adaptive Wafer Scale Integration (AWSI) is a concept which originated in late 1971 at McDonnell Douglas Corporation.[1] It employs electrically alterable, nonvolatile interconnect controller circuits processed into a semiconductor wafer to connect "arrays" of interconnected, operable circuits (also processed into the wafer) to a bus structure deposited on the wafer between the arrays. With this approach, AWSI can have important advantages relative to other high density electronic circuit approaches. Such advantages potentially include: repeated electronic reconfigurability of interconnected circuits, compatibility with a wide variety of semiconductor processes, ability to select for yield, improved reliability, self-healing and fault tolerance; plus reduction in size, weight, and cost.

The technological basis for the AWSI interconnect is the nonvolatile semiconductor memory transistor, the MNOS, (metal-nitride-oxide semiconductor).[2-4] The MNOS transistors, utilized in a circuit, effectively became the means with which electrically alterable interconnection can be implemented in place of hardwired interconnections.[5-9] This alterable interconnect is possible because interconnection is controlled by a nonvolatile memory so that its state is static as if hardwired. Yet it is alterable (that is adaptive), via control signals by circuit means.

As an introduction to the AWSI concepts in concrete physical terms, we can use as an example an early feasible demonstration vehicle, the RMWC-1. The interconnect is composed of an electrically alterable, nonvolatile, MNOS memory cell and a standard logic or buffer gate MNOS transistor circuit or bus controller. The bus controller is enabled by an enable signal which is conditional on the stored interconnect status of the memory cell. The bus controller gate, the power, clock and data signals from the interconnecting bus to the engaged circuit, in this case, a shift register. The relationship of the MNOS memory cell, the bus controller and the shift register in the AWSI implementation is shown in Figure 1.

This particular example circuit has been fabricated and integrated on a wafer; the data path organization is illustrated in Figure 2. It may be seen that a shift register in a given horizontal string may be either connected in series with the data line or bypassed.

In the nonvolatile mass memory, the application of AWSI is further extended. On-the-wafer interconnect is mechanized such that small single-chip sequential access memory arrays (with memory storage chip capacity in the range of 4k to 8k bits per memory array) are interconnected to result in a large capacity store (on the order of 10^6 bits) in a wafer. The use of nonvolatile memories as the storage array in a mass memory system results in very low system power

as compared with other memories implemented with RAM's or CCD's. Power need be applied only to those storage arrays accessed with no standby power necessary to maintain data in unaccess storage arrays.

A 4096 bit nonvolatile sequential access memory (SAM) was developed as the basic memory storage array.[10] Several features of the SAM array uniquely establish its application in an AWSI memory: (1) Memory storage is nonvolatile, based on N channel MNOS storage. (2) Data input is high impedance and buffered with an input latch; data output is tri-state, and buffered for bus driving. (3) To reduce interconnect bus lines, access within the SAM storage array is sequenced internally, timing input is restricted to a single clock line, and operation instructions are decoded internally. (4) For multiplexed operation in a bus interconnected system, a chip select control and a flag bit are provided.

The mechanization of on-the-wafer interconnect is accomplished with the development of associative interconnect. The associative interconnect consists of 6 major components: (1) the macrobus which is the system bus, (2) power switches, (3) power connect/disconnect logic, (4) nonvolatile address memory, (5) address memory control, (6) address comparators.

The memory array wafer, MAW, was designed with the SAM storage array and interconnected using the associative interconnect. The successful operation of MAW points the way to AWSI magabit memory modules for bulk store application.

1. W. A. Geideman and A. L. Solomon, "Wafer Integrated Semiconductor Mass Memory," Int. Telemetering Conference, Los Angeles, California, Nov. 1978.
2. H. A. R. Wegener et al, "The Variable Transistor, a New Electrically-Alterable Non-Destructive Read-Only Storage Device," Int. Electron Device Mtg., Washington, D.C., Oct. 1967.
3. M. H. White and J. R. Cricchi, "Characterization of Thin-Oxide MNOS Memory Transistor," IEEE Trans. Electron Devices, Vol. ED-19, pp. 1280-1288, 1972.
4. Y. Hsia, "Cross Gate MNOS Memory Device," IEEE Trans. Electron Devices, Vol. ED-25, pp. 1071-1072, 1978.
5. R. L. Petritz, "Current Status of LSI Technology," IEEE J. Solid State Circuits, Vol. SC-2, pp. 130-149, Dec. 1967.
6. D. F. Calhoun, et al, "Status and Future Direction of Pad Relocation Full Wafer LSI," IEEE Elec. Comp. Conference, 1973.
7. J. C. Hunter, "Data Base Retrieval Using Superchips," Symposium on Advanced Memory Concepts, Stanford Research Institute, Menlo Park, California, June 1976.
8. R. C. Aubusson and I. Catt, "Wafer Scale Integration - A Fault-Tolerant Procedure," J. Solid State Circuits, Vol. SC-13, pp. 339-344, June 1978.
9. Y. Egawa, et al, "A 1 Mb Full Wafer MOS RAM," IEEE Int.Solid-State Circuits Conf., 1979.
10. R. Rodgers and Y. Hsia, "A 4K-Bit N-Channel MNOS Sequential Access Memory," Presented at the 1979 IEEE NVSM Workshop, Monterey, California, March 1979.

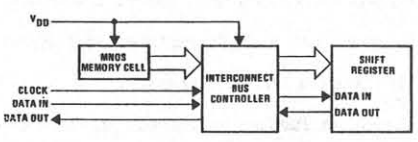

Figure 1
Use of AWSI to Interconnect a Shift Register String

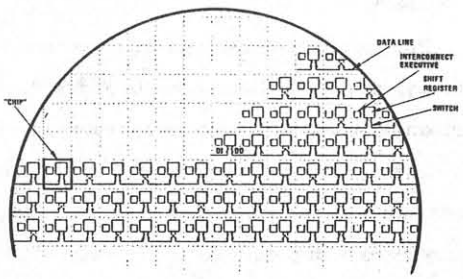

Figure 2
Data Path Organization of RMWC-1