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A 3000-Gate CMOS Masterslice LSI

M.Ashida, R.Hoshikawa, N.Matsumura, J.Ishii, H.Ichikawa, Y.Sugiura, K.Inayoshi

Fujitsu Limited, IC Division

1015, Kamikodanaka, Nakahara-ku, Kawasaki, Kanagawa, 211, Japan

This paper will describe a low-power masterslice which can take up to 3000 effective gates without any special cooling requirement. The masterslice adopts silicon-gate CMOS of 3.6 μm gate length and double layer metal interconnection process.

The features of the LSI are summarized in Table-1. The masterslice has 3900 basic cells as a matrix of 150 x 26, and 72 I/O cells on chip periphery. An overall view of the chip is shown in Figure-3. Circuit and layout of the basic cell are shown in Figure-1. This basic cell configuration simplifies the construction of various unit cells, which have specific logic functions, through specific contact and metalization patterns.

The unit cells are fundamental logic unit to start with a logic design. About 60 types of unit cells are prepared for logic designers. The switching characteristics of 3 types of unit cells are listed in Table-2 for example. Figure-2 is a photograph of the D-type flip-flop corresponding to the unit cell C in Table-2.

Two layer metal interconnection technique permits to confine the high resistivity poly-silicon wirings into the small region of basic cell columns, then the propagation delay caused by long poly-silicon wiring can be eliminated. Electrically characterized unit cell family and this 2 layer metal wiring technique made possible to realize good control and accurate prediction of delay time of the circuit used in the LSI. Thus logic designers can reasonably analyze the delay time of critical paths and can confirm the performance of the circuit resulted from actual layout through suitable DA support. And possibility of malfunctions of LSI's due to large deviations of circuit delay time were considerably reduced in this masterslice technique.

Physical routings among unit cells as well as between unit cells and I/O cells are made not only in reserved wiring area but also unused channels across the basic cell columns.

Using this masterslice, several custom LSI's have been fabricated. Figure-3 is a photograph of the chip for disk device controller (DVC). This LSI uses 3756 basic cells, and corresponds to 405 TTL SSI/MSI packages. An average propagation delay time of DVC chip is around 7 ns, and power dissipation is about 50 mW at 10 MHz operating frequency. Figure-4 demonstrates a comparison between calculated

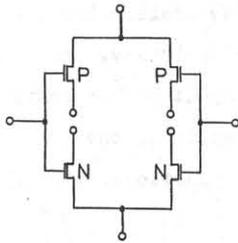
and measured propagation delay time of a logic chain in the LSI fabricated in this work.

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* No. of basic cells	3900
* No. of I/O cells	72
* Chip size	9.72 x 9.72 mm ²
* Power supply	5 V
* Logic level	TTL
* Propagation delay time	
Internal gate	7 ns (average)
Output buffer	20 ns (60pF load)

Table-1 Features of LSI



(a) Circuit

	No. of BC's	t _{up}		t _{down}	
		t ₀ (ns)	k _{CL} (ns/lu)	t ₀ (ns)	k _{CL} (ns/lu)
A. 2 Input NAND	1	1.5	1.02	4.2	1.00
B. 2 Input NOR	1	1.8	1.98	2.8	0.63
C. D-type FF	7	15.8	1.02	13.0	0.63

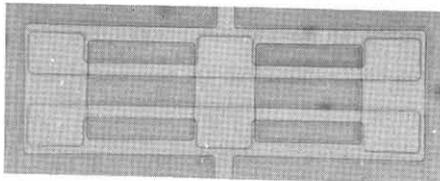
BC ; Basic cell

1 (lu) = Capacitance of one input of BC

$$\text{Propagation delay time} = t_0 + k_{CL} \times C_L$$

(t_{up}, t_{down})

C_L ; Sum of wiring capacitance and fan/in capacitance of unit cells



(b) Layout

Figure-1 Basic cell

Table-2 Switching characteristics

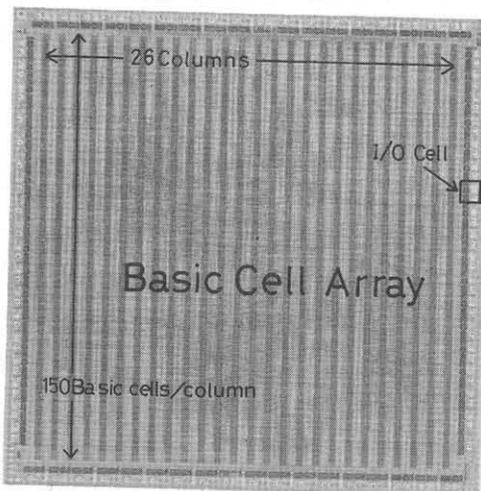


Figure-3 Photograph of the chip

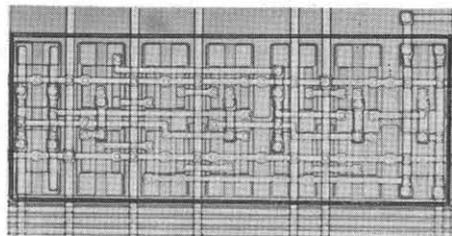


Figure-2 Photograph of unit cell (D-type FF)

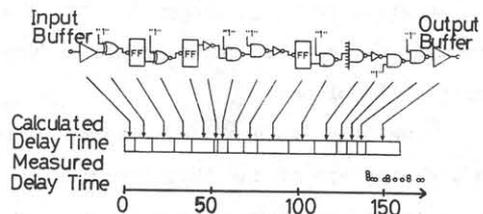


Figure-4 Calculated and measured propagation delay time