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Effects of High Temperature Hydrogen Annealing on n-channel Si-gate MNOS Devices.

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In recent years, electrically erasable programmable read only memories (EEPROM's) have become the subject of intensive research.[1)-3)] Conventional MNOS memory devices, which are currently used as EEPROM's, have some distinct disadvantages, such as low speed and low packing density, due to their p-channel Al-gate structures. Although n-channel Si-gate MNOS devices have the potential for significantly higher speed and packing density, it has been difficult to realize Si-gate MNOS devices with high performance because memory retention is degraded by high temperature annealing in nitrogen,[4)] which always accompanies the Si-gate process.

This paper makes it clear that the degradation of memory retention depends strongly on the annealing ambient and that high temperature hydrogen annealing is very effective for improving memory retention. This can be used as an essential technique for fabricating n-channel Si-gate MNOS type EEPROM's.

An outline of the process used for fabricating 2K and 16K EEPROM's[5)6)] is given in the flow chart in Table I. In the process sequence, the structure is annealed in H_2 at high temperature after PSG (Phospho-Silicate Glass) deposition. This H_2 annealing not only improves memory retention but also makes the PSG layer more dense, activates the phosphorus ions implanted in the source/drain region, and stabilizes the MNOS and MOS structures.

Results of memory retention measurements are shown in Fig.1. Samples (A),(B) and (C) were annealed in N_2 at 800, 900 and 1000°C, respectively. Sample (D) was annealed in H_2 at 800°C. These results show that high temperature H_2 annealing has a remarkable effect in increasing memory retention, particularly in the negative threshold voltage region, even though N_2 annealing causes degradation of memory retention.

Some experimental results of low frequency C-V curves obtained from quasi-static measurements are shown in Fig.2 in order to clarify the relation between memory retention and interface states. Measurements were performed on MNOS capacitors prepared as follows: thin SiO_2 and Si_3N_4 layers were successively formed on a lightly etched p-type (100) wafer and annealed in N_2 or H_2 then Al gates were formed. The interface state density N_{ss} is decreased markedly to about 10^{10} cm^{-2} by H_2 annealing at 1100°C for 20 min, while the N_{ss} of the sample annealed in N_2 at 800°C for 20 min is about 10^{11} cm^{-2}.

From these results, the mechanism of memory retention improvement by H_2 annealing is speculated to be as follows: high temperature H_2 annealing results in decrease of slow interface states which locate in the vicinity of the oxide-silicon interface, thereby decreasing the decay rate of the charge stored near the oxide-nitride interface. Moreover, the slow interface state should be ionized negatively and become able to capture hole. This is why the effect of H_2 annealing on memory retention is distinct in the erase state with negative V_{th} values as previously shown in Fig.1.

It should be noted that to obtain the excellent memory retention, the temperature of the H_2 annealing has to be the highest of all temperatures to which the wafers are exposed after nitride deposition. High speed and largely integrated 16K EEPROM's such as that shown in Fig.3 have been fabricated using this technique.

Conclusions

1) High temperature H_2 annealing improves MNOS memory retention remarkably.
2) The improvement of memory retention is due to a decrease in the slow interface states in the vicinity of the oxide-silicon interface.
3) This key processing technique has realized advanced EEPROM's which consists of n-channel Si-gate MNOS memory devices.

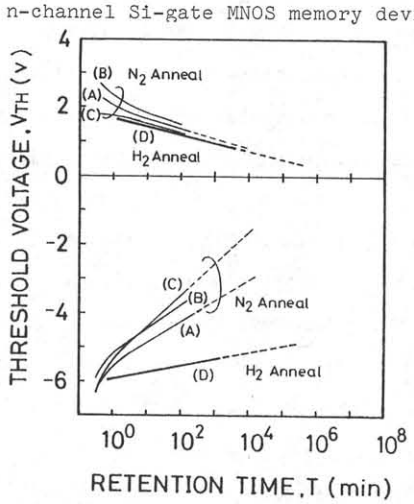

Fig.1 Retention characteristics of n-ch. Si-gate MNOST's.

Table I Process flow chart

1. Starting material; 8-12 ohm-cm, (100), n-type
2. Well structure formation
3. Oxidation for isolation
4. Formation of peripheral MOS
5. Formation of MNOS
6. Phosphorus ion implantation for source/drain
7. PSG deposition
8. High temperature H_2 anneal
9. Al metallization
10. Sinter metal (H_2 at relatively low temperature)

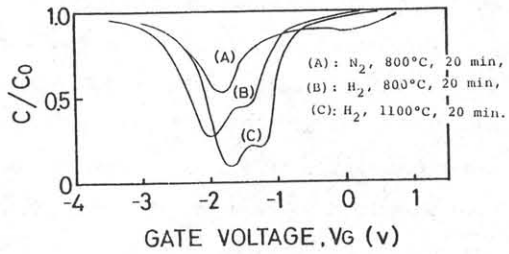

Fig.2 Low frequency C-V curves.

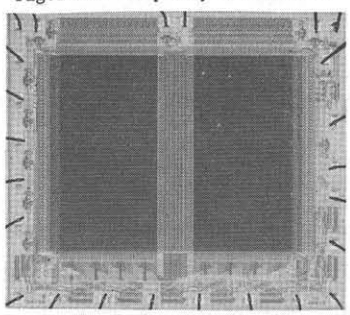

Fig.3 Microphotograph of the 16K EEPROM chip: size is 4X4.5 mm^2.

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