Digest of Tech. Papers The 11th Conf. (1979 International) on Solid State Devices, Tokyo N-channel High Speed Nonvolatile Static RAM Utilizing MNOS Capacitors S.Saito, Y.Uchida and N.Endo Semiconductor Device Engineering Lab. Toshiba Corporation, Kawasaki, Japan

A - 5 - 5

Previously we reported about 256-bit and lK-bit P-channel nonvolatile semiconductor read write RAM (1)(2), by introducing the nonvolatile static RAM cell as shown in Fig.1(a). This type of RAM is featured by highly reliable nonvolatile RAM operation, but there still remain several problems such as, low bit density, and requirement of 2 kinds of power supplies (+5V,-15V).

The purpose of this paper is to propose an improved nonvolatile static RAM with higher bit density, and higher speed with only single 5V power supply.

We introduce a new nonvolatile RAM cell as shown in Fig.1(b). This memory cell consists of N-channel MOS flip-flop circuit constructed by 6 MOS transistors and a pair of N-channel MNOS capacitors MCl and MC2, each of which is connected to one of the bistable nodes Q and \overline{Q} . The schematic structure of the N-channel MNOS capacitor is shown in Fig.2. This MNOS capacitor can be operated as the variable threshold switching capacitor as shown in Fig.3, which switches at an threshold voltage of eiter $V_{\rm THO}$ or $V_{\rm TH1}$ depending upon the previously applied voltage.

Memory operations of this new cell are as follows: Under stable power supply, this cell can be operated as the conventional MOS static memory cell with high speed. The nonvolatile memory operation can be attained by applying the erasing and writing voltage pulse to the MNOS gate signal line MG. By the erasing pulse, both threshold voltages of paired MNOS capacitors shift to the low level $V_{\rm TH0}$. And when the writing pulse is applied, one of the MNOS capacitors whose source voltage is at the $V_{\rm SS}$ level changes its threshold voltage to the high level $V_{\rm TH1}$. On the other hand, the other maintains its low threshold state $V_{\rm TH0}$ because of large inhibiting voltage self-generated at the floating node by bootstrapping effect through the MNOS capacitor. By applying a read pulse signal to the MG line, the information of the paired MNOS capacitors in the form of threshold difference is retrieved into the flip-flop circuit through the capacitive sharing mechanism between the MNOS capacitors and the stray capacitors at the nodes.

A 16-bit fully decoded nonvolatile static RAM IC were designed and fabricated utilizing a combination of N-channel Si-gate MOS technology and N-channel Al-gate MNOS technology to verify the performance of the new cells experimentally. The microphotograph of the chip is shown in Fig.4. Typical MNOS read margin characteristics versus MNOS writing voltage are shown in Fig.5. Fig.6 shows typical memory retention characteristics of the N-channel MNOS structure at room temperature.

Consequently, basing upon this technology, the estimated cell area should be as small as $2000 \mu m^2$ using 3-4 μm design rule which is almost 1/6 of the previous cell area, therefore we will be able to realize nonvolatile static RAM of 4K-bit or beyond, which operates with the access time of less than 100ns under a single 5V power supply except for MG signal, and whose retention time shall be more than 1 year at room temperature.

Acknowledgement: The authors wish to thank Mr.M.Misumi and Mr.K.Tokushige for their supports in experiment, and Mr.K.Hashimoto, Mr.S.Morita and Miss. K.Aizawa for their suppots in fabrication process, and Dr.Y.Nishi, Dr.H.Iizuka, Dr.H.Hara, Dr.T.Sato, Dr.S.Mimura and Mr.M.Nakane for their helpful discussions. Reference

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Fig.l Circuit configuration of memory cells. (a) prior circuit (b) new circuit



Fig.4 Microphotograph of 16-bit nonvolatile Fig.3 Schmatic switching static RAM IC chip.







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Source

Gate

AL

SiO2 (~20Å)

P-Type Silicon

MNOS capacitor.

MC, or MC

Si3N4(~550Å)

characteristics of MNOS capacitor.



