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Dynamic Injection MNOS Memory Devices

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On the basis of the N-channel Si-gate MNOS fabrication process[1], a new MNOS structure is proposed which features high-speed writing, single 5 V drain voltage, and the potential capability of integration with other circuits.

Two basic structures are shown in Fig. 1(a) and (b). They have one or two control gates (enhancement MOS transistors) and an MNOS memory between control gates and field SiO_2 layer.

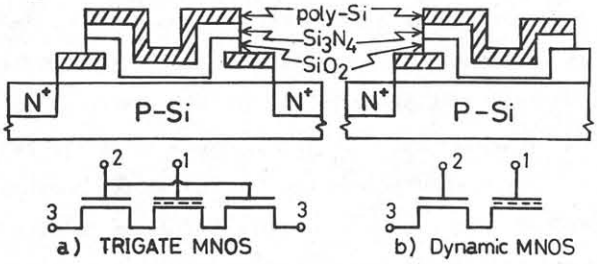

Fig. 1 Cross sections and equivalent circuits

In the above structures, the inversion layer under the MNOS gate is filled with charge transferred from the source through the control gate while writing voltage is applied to the MNOS gate. Then, the control gates are electrically closed and the stored charge in the inversion layer is injected into the interface of the thin SiO_2 and Si_3N_4 layers in the MNOS.[2),3)] Injection is completed in a much shorter time than the minority carrier storage time, so no writing occurs in the absence of the signal charge. This device has been named Dynamic Injection MNOS (DIMNOS) because of these operating characteristics. It has the following unusual features:

1) Writing can be done without the waiting time which conventional nonvolatile memories require. Therefore, writing time can be greatly reduced if DIMNOS is used in a large scale memory array.

2) DIMNOS can be operated by a single 5 V source, except for the high writing voltage applied to the MNOS gate. That is, application of high voltage to a drain region[1] is not necessary in DIMNOS, as write-inhibition is attained by cutting a channel under the control gate.

3) Dynamic Random Access Memory (Dynamic RAM) with MNOS backup on the same chip can be realized with small cell size, less than 400 μm^2.

In the write mode, DIMNOS devices are operated in the following sequence, as shown in Fig. 2.

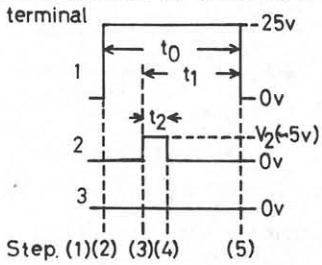

Fig. 2 Timing sequence in DIMNOS

Step(1) All terminals are set to 0 V,
Step(2) Terminal 1 to writing voltage of 25 V,
Step(3) Terminal 2 (of the cells to be written) to about 5 V,
Step(4) Terminal 2 to 0 V, and
Step(5) Terminal 1 to 0 V.

In Step 2 the Si surface of the MNOS is depleted and most of the writing voltage is added between the Si surface and substrate so that the MNOS memory can not be written. In Step 3, electrons are transferred to the Si surface of the MNOS and an inversion layer is formed on the surface. Even when Terminal 2 is set to 0 V in Step 4, stored charges in the inversion layer cannot escape and the MNOS memory continues to be written until Terminal 1 is set to 0 V. Therefore, the MNOS memory is written within the time from Steps 2 to 5, which is less than 1 msec. In a large scale DIMNOS memory, all bits can be written in parallel, simply repeating Steps 3 and 4 for each word line. In this case, the total writing time is determined only by the time necessary for Steps 3 and 4, which is less than 50 nanosec, multiplied by the number of words. In the read and erase modes, the device shown in Fig. 1(a) is operated in the same way as described in ref. 1.

Experimental results for the device shown in Fig. 1(a) are shown in Figs. 3 and 4. Writing is indeed inhibited for writing pulse widths t_0 shorter than 10 msec if number of inhibited writing attempts is less than 10 as is shown in Fig. 3. When V_2 is greater than 1.0 V, the MNOS memory is fully written in less than 50 nanosec, which is almost the same as conventional MNOS memory devices[1] (see Fig. 4).

The device shown in Fig. 1(b) can be operated normally as a 1 transistor dynamic RAM while the MNOS memory is erased. When external power is removed, information in the stored capacitor is temporarily stored in a peripheral flip-flop circuit connected to Terminal 3 by the read operation, and then written in the MNOS memory by "dynamic injection" for each word line. When the power is restored, the information in the MNOS is retrieved and transferred back to the stored capacitor by repeating the read and word erase operations for each word line.

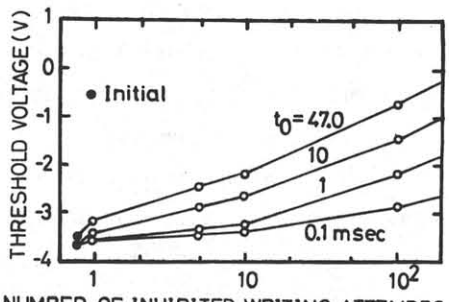

Fig. 3 Write-Inhibit characteristics

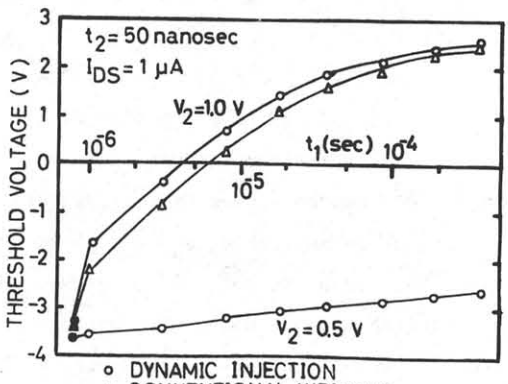

Fig. 4 Writing characteristics in DIMNOS (V_{th} in control MOS tr. is 0.7 V)

Characteristics and operation limits of DIMNOS are discussed in detail, together with the fabrication process and peripheral circuits.

1) Y. Yatsuda et al., The 10th Solid-State Conference, 21 (1978).
2) K. Goser et al., IEEE J. of Solid-State Circuits, SC-9, 148 (1974).
3) M. H.White et al., IEEE J. of Solid-State Circuits, SC-10, 281 (1975).