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A—5—8 MNOS Traps and Tailored Trap Distribution Gate Dielectric MNOS

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There have been many investigations[1-8] into the MNOS device physics, the properties of the memory traps and the role of the gate dielectrics on device behaviors. Much valuable information has been gathered, but there is the conspicuous absence of a microscopic model that can correlate the known facts. We propose such a model that identifies the memory traps as silicon dangling bonds or equivalently incompletely bonded silicon in the silicon nitride. A silicon dangling bond that has an electron in it is electrically neutral. The energy level for this electron is inside the energy gate of Si, at an energy D_o, slightly below the mid-gap positions, as illustrated by the electron energy diagram of a MNOS structure in Figure 1. However, this neutral configuration of the dangling bond has not the lowest energy. Instead either of the two charged configurations, one with the dangling bond possessing two electrons and the other with the same possessing none (i.e. two holes), are lower in energy. Hence the system of Si dangling bonds cooperatively lower their total energy by electron charge transfer from one dangling bond to the other. Such charge transfers are accompanied by bond distortions. The result is the formation of positively and negatively charged dangling bonds replacing the neutral original ones. The negatively charged dangling bond state D^-, with two electrons, lies in energy below D_o, near the Si valence band edge. D^- is a hole memory trap. The positively charged dangling bond state D^+, with two holes, lies in energy above D_o, near the Si conduction band edge. D^+ is an electron memory trap. If the initial charge state of the silicon nitride film is neutral, then we must have equal numbers of D^+ and D^- states compensating each other. Since these memory traps D^+ and D^- are charged, the large observed capture cross-section of $5 \times 10^{-13} cm^2$ is not unexpected. The trap center is amphoteric, i.e. the dangling bond can possess either of the two charge states, D^+ or D^-.

In CVD nitrides large amounts of H are incorporated and bonded to either N or Si. The interplay of our charged dangling Si bonds with the Si-H bonds have been considered in particular with respect to high temperature anneal of low temperature nitride, and the effects of write/erase cycling.

Our model of memory traps enables us to identify what are the desirable chemical composition of the nitride for optimization of memory device parameters including endurance, retention and window size. It turns out that the competing properties of the traps present a formidable task to optimize the several desired properties of an MNOS transistor. For example the existence of a large trap concentration in the dielectric enhances memory window, but the very large trap concentration facilitates transport of charges which leads to poor memory retention; and,

as another example, the use of hydrogen to passivate fast surface states leads to availability of excess Si-H bonds susceptible to band breakage with stress from endurance cycling.

To exploit the understanding brought forth with the trap model, the nitride dielectric can be structured for a specified trap distribution by vertically grading the nitride film via film deposition processes. To illustrate, in Figure 2, we observe the relationship of threshold window decay to the influence of traps in the nitride dielectrics. Nitride fabricated with large trap density (curve A) exhibits a large V_T shift (for low conductance state of an MNOS memory transistor) with corresponding large retention decay, while the opposite holds true for nitride fabricated with low trap density. In curve C, an optimized MNOS retention feature is accomplished with a triple layer dielectric in which backward charge transport is minimized and sufficient traps exist in the nonimmediate regions of the dielectric for threshold shift to enhance MNOS memory window.

1. E. C. Ross and J. T. Wallmark, RCA Rev. 30, 366,(1969).
2. M. H. Wood and J. W. Tuska in Proc. 10th Reliability Physics Meeting 120, (1972).
3. S. Zirinsky, J. Elect. Matls. 4, 591 (1975).
4. C. A. Neugebauer and J. F. Burgess, J. Appl. Phys. 47, 3182, (1976).
5. M. H. White, J. W. Dzimianski and M. C. Pekerav, IEEE ED-24, 577, (1977).
6. K. O. Jeppson and C. M. Svensson, J. Appl. Phys., 48, 2004, (1977).
7. N. Endo, Solid State Electronics, 21, 1153, (1978)
8. Y. Hsia, W. W. Y. Lee, Y. J. Chen and K. L. Ngai, Presented at 36th Annual Device Research Conf., Santa Barbara, CA, (1978).

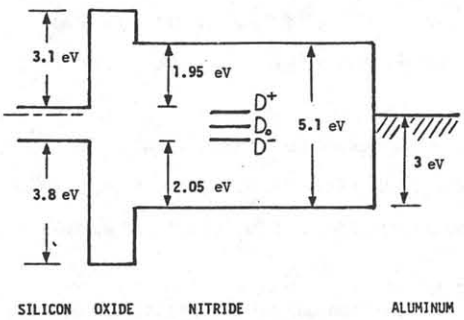

FIGURE 1 ELECTRON ENERGY DIAGRAM OF MNOS STRUCTURE

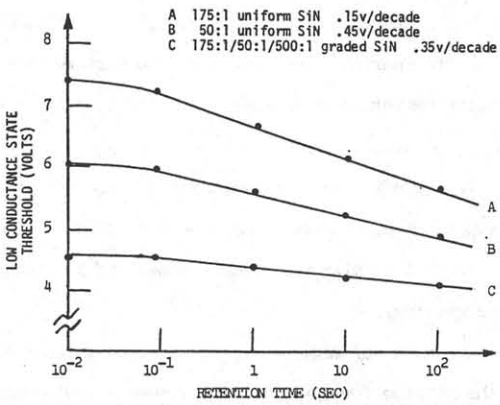

FIGURE 2 MNOS RETENTION VS SiN COMPOSITION