

A—6—10 Transient thermal simulation and its use in power IC design

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Introduction - Thermal effects may represent a limiting factor in the development of IC's. Therefore, as the power dissipated by integrated circuits becomes more relevant, the need increases for accurate modeling of the static and dynamic thermal behaviour of the die-package structure.

An accurate three-dimensional modeling of the transient thermal profile following the application of a step in power dissipation is particularly needed when the IC designer is willing to take advantage of the thermal transient to realize a time-modulated thermal protection of the power transistor using the time-varying thermal gradient, or a delay of the order of a fraction up to a few milliseconds, without using external components.

In this paper, we first report on the analytical solution of the transient thermal diffusion problem, in three dimensions for a two-layer structure, and show a thermal transient solution for a 25 W step power function; in the second part, we report on a new power IC with time-modulated thermal protection, designed with the help of the thermal simulator.

Transient thermal simulation - Transient thermal profiles on the chip can be obtained solving the classic heat-flow problem: $\nabla^2 T(x,y,z) = D^{-1} \frac{\partial T}{\partial t}$, where the coefficient D is assumed constant with T. The need for a three-dimensional solution is due to the fact that the IC chip is a three-dimensional structure, as opposed, for example, to the fingers of discrete transistors, which can be considered infinitely long. Basically, two methods can be used to solve the above equation: the purely numerical method and the analytical approach. Computer programs based on the finite difference method are quite large, require a large memory and long computation times for a reasonable accuracy.¹ The analytical approach permits a drastic reduction in program size, CPU time, and the algorithm can be easily implemented on a minicomputer.² In order to obtain the analytical solution, the actual structure of the small silicon chip on a large copper substrate has been simplified to a two-layer structure with equal dimensions (the z-axis is considered perpendicular to the silicon surface, pointing towards the copper substrate); such geometrical simplification is acceptable, since most of the heat certainly flows through the portion of the substrate directly below the silicon chip. A computer program computes the three-dimensional transient solution in T, given the physical and geometrical characteristics of the structure and the power distribution $P(x,y,0)$; generally, such $P(x,y,0)$ is given as a pattern of box functions located at the power transistor sites. The program computes the transient thermal profile for $z=0$ (chip surface), which represents the most common information required; however, it is also possible to specify a z (distance from the top surface) at which to compute the temperature, for example at the silicon-copper interface.

Our solution represents a new analytical result, since existing solutions proposed in the literature consider either a uni-dimensional and semiinfinite structure,³ or only the thermal transfer function and not the function $T(t)$.⁴ Figure 1 shows a plot of the chip surface temperature vs. distance x, at different times for a step input power of 25 W; the temperature is computed along the section where the temperature is highest. On the x-axis, the black region indicates the position of the dissipating power transistor.

Application to a 6A current booster - In this section, we present the design of a 6A current booster (TDA 1490) where the short-circuit protection is based upon the transient behaviour of the thermal gradient, as indicated by the simulation techniques described previously. Two devices, a transistor and a diode, are the active temperature sensors of the short-circuit protection. They are placed at a suitable distance from the power transistor; another suitable distance exists between them, such that the sensors act upon the short-circuit current according to the transient of the thermal gradient existing between them.

The distance between the power transistor and the first sensor determines the time during which the maximum current (6A) can be tolerated according to the SOA of the power transistor. The distance between the first and second sensor determines the amount of reduction in the maximum current due to the thermal gradient existing between the sensors. The position of the sensors in the layout, being closely related to the thermal profiles, has been optimized using the simulation technique described earlier.

Figure 2 shows the oscillograph of the short-circuit current vs. time (Hor: $500\mu\text{s}/\text{div}$; Ver: $1\text{A}/\text{div}$). The protection limits the current to 6A for a very short time before lowering it to 3A. With such delayed protection the booster can drive an inductive load without showing the dangerous voltage spikes on the output waveform.

References

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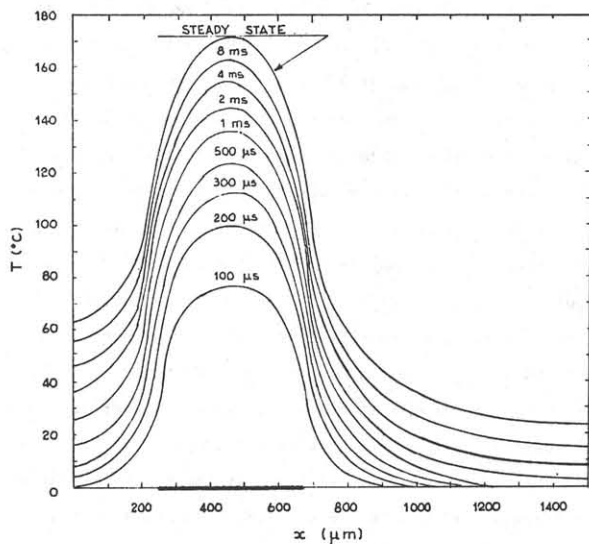


Fig. 1

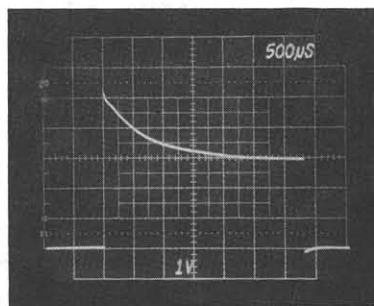


Fig. 2