#### Digest of Tech. Papers The 11th Conf. (1979 International) on Solid State Devices, Tokyo

# A-6-12 A 100 W Static Induction Transistor Operating at 1 GHz

Y.Kajiwara, M.Aiga, Y.Higaki, M.Kato, Y.Yukimoto and K.Shirahata Semiconductor Laboratory, Mitsubishi Electric Corporation.

4-1 Mizuhara, Itami, Hyogo, 664 JAPAN

### INTRODUCTION

The demands of microwave high power solid state devices have been increasing in the communication and consumer electronics. A static induction transistor  $(SIT)^{(1)}$  has been the most promising device for high power and high frequency operation.<sup>2),3),4)</sup> The SIT is a majority carrier device and its negative temperature coefficient of drain current prevents the SIT from thermal run away. A 100 W SIT operating at 1 GHz in CW has been realized by a fine patterning technique and a new internal matching technique. EXPERIMENTAL

Two impotant techniques were improved to realize the 1 GHz 100 W SIT. One was the fine patterning technique and another was the power combination technique. The power gain increases with  $Gm/C_{DG}$ . Where, Gm is the mutual conductance and  $C_{DG}$ is the capacitance between drain and gate. To raise the power gain, it is most effective to reduce  $C_{DG}$  by compression of the area of the active region in the SIT chip. Very fine source patterns with 1 µm width and total length of 16.6 cm in an SIT chip were fabricated by conventional photolithography. Silicon wafers were taken care to be prevented from waving or bending. The thickness of the photoresist and exposure condition were strictly controlled.

To obtain higher output power, a parallel operation of multiple chips and even power sharing are indispensable. An SIT chip includes 5 transistor blocks. In the 1 GHz 100 W SIT, 10 transistor blocks were combined. The input matching networks and shunt inductors as the output matching networks were connected to every block, as shown in Fig. 1. Usually, a brief network has been attached for output matching. These internal matching networks to every transistor block made the even power sharing.

By the multiple blocks operation of 4, 6 and 10 blocks, the output powers of 40, 59 and 101 watts at 1 GHz were obtained, respectively, as shown in Fig. 2. While the output power of 10 watts with gain of 7 dB was obtained by one block operation. At the output power of 100 watts, the power gain was 4 dB and the drain efficiency was 40 %. The input and output impedances of the internally matched SIT combined with 10 blocks were 3.1-j3.5 ohm and 5.3+j1.3 ohm at 1 GHz, respectively. By the internal matching to every block, the power of 10 blocks were well combined and output power of 100 W was obtained with high gain.

-195-

## CONCLUSION

A 1 GHz 100 W SIT has been realized. A gain of 4 dB and an efficiency of 40 % at the output power of 100 watts were obtained, by the excellent fine patterning and power combination techniques.

## ACKNOWLEDGMENT

The authors are grateful to professor J.Nishizawa of Tohoku University for his technical discussion. They also thank to Dr. T.Kitsuregawa of Mitsubishi Electric Corp. for his encouragement.

### REFERENCES

1)	J.Nishizawa	a e	t al	Ĺ. (	; IEEE Trans. ED-22, pp 185-197, (1975).	
2)	Y.Kajiwara	et	al	;	IEEE MTT-s 1977 International Microwave Symposium, Tech. Digest, pp 281-284.	
3)	Y.Kajiwara	et	al	;	7th European Microwave Conference 1977, Tech.Digest, pp 629-633.	
4)	Y.Kajiwara	et	al	;	IEEE MTT-s 1978 International Microwave Symposium, Tech. Digest, pp 380-382.	











Fig.2 Amplifying characteristics of SITs combined with multiple blocks at 1 GHz.