A—6—13 A New Transistor with Improved Safe Operating Area

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Second breakdown in high power bipolar transistors is a major limitation on the safe operating area (SOA). A multi-emitter transistor, ballasted with series resistance for each emitter diode, was proposed to increase the SOA. However, the SOA for reverse base drive operation was not improved.[1)]

Gate associated transistor(GAT)[2.3)] was found to have large SOAs for both forward and reverse base drive operations using an optimum gate structure. In this paper, a high power GAT for high frequency use with an improved SOA was proposed and the mechanism for the improvements in SOA was clarified.

Figure 1 shows a cross section of GAT. The details of the GAT was already reported.[2.3)] GATs were fabricated with a maximum oscillating frequency of 350 MHz, collector to emitter breakdown voltage (BV_{CEO}) of 220 volts, and a collector current (I_C) of 10 amperes.

The SOA for forward base drive operation was investigated by measuring junction temperature rises against emitter current and power dissipation in the transistors. Figure 2 shows a relation between junction temperature and emitter current of GAT compared with a conventional transistor. The emitter current at which junction temperature rises suddenly was about 2 times as large as in the GAT compared with the conventional transistor. Figure 3 shows a relation between collector current and collector to emitter voltage V_{CE} corresponding to the junction temperature of 125°C. The data shown in the range of V_{CE} larger than 100 volts corresponded to the destruction of the transistors at that collector current I_C. The SOA of the GAT was clearly larger than that of the conventional transistor.

SOA for reverse base drive operation was investigated by measuring a relation between I_{CEO} and V_{CE} of GAT and conventional transistor, as shown in Fig.4. Collector to emitter breakdown voltage for open base operation BV_{CEO} of GAT was 2 times as large as that of the conventional transistor having f_{max} of 350 MHz.

For the forward base drive operation, the SOA is limited by excessive localized temperature rise due to the current concentration at the edge of the emitter (current crowding effect), which is characterized by an effective emitter width (L_{eff}) given by eq. 1.[4)]

$$L_{eff} \simeq \frac{2kTW'}{q(1-\alpha)\rho_b} \cdot \frac{h}{I_e} \qquad (1)$$

where k is Boltzmann constant, T absolute temperature, q electron charge, W base width, ρ_b base resistivity, h emitter length, I_E emitter current, α current gain.

Because gates of GAT were diffused deeper and with higher impurity concentration than base region, they make W and β_b larger and smaller, respectively, than those of the conventional transistor. Effective emitter width L_{eff} of the GAT was, therefore, larger than that of the conventional transistor and reduces the current crowding effect in GAT.

For the open base or reverse base drive operation, the SOA is limited by avalanche injection which occurs when high current density and high electric field are simultaneously present in the collector region. The multiplication factor in avalanche breakdown and BV_{CEO} were theoretically calculated by considering gate shielding effect for various gate structures and for a conventional transistor. The results of Fig. 4 was obtained for the optimum gate structure and coincided with the calculated results. From these results, gate shielding effect seems to reduce multiplication factor in avalanche breakdown and suppress avalanche injection.

In conclusion, GAT having 2 times as large as safe operating area compared with conventional transistor was fabricated by optimizing gate structure for high power and high frequency use. The gates suppress current crowding and reduce multiplication factor in avalanche breakdown for open base or reverse base drive operation.

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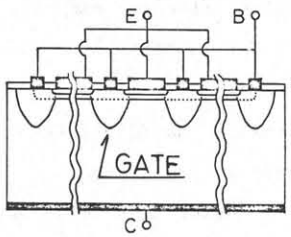

Fig.1 Cross section of GAT

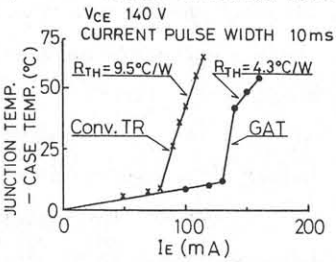

Fig.2 A relation between junction temperature and emitter current

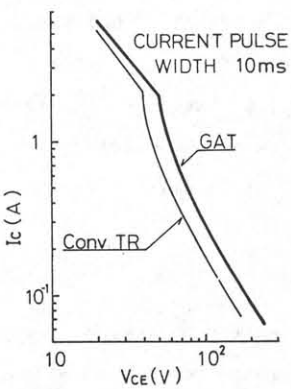

Fig.3 A relation between I_C and V_{CE} corresponding to the junction temperature of 125°C.

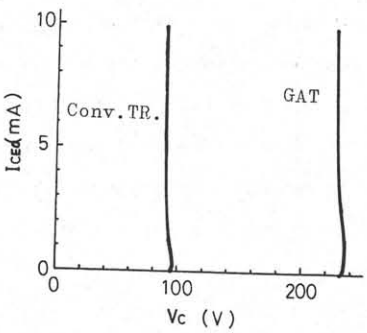

Fig.4 I_{CEO} vs. V_{CE} characteristics