A — 6 — 2 A New Multiplex Input Technique For High Density CCD Memory

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To obtain high density CCD memory, sense amplifiers must be laid out effectively. In this meaning, several channels are multiplexed to one sense amplifier. In this paper, we present a new multiplex input technique utilizing charge splitting operation. By using this new technique, a 64K-bit CCD memory has been designed and operated successfully.

The writing operation by the charge splitting method is illustrated in Fig. 1, which shows the cross section and surface potential along input stage. The input stage consists of "input gate" (I gate), "holding cell" (H cell), "coupling cell" (C cell) and "splitting gate" (S gate). Prior to setting data on the input node, the I gate and H cell are automatically filled with charge at time T1 (Fig. 1). The signal, "1" or "0", is injected into the H cell (time T2). For writing a "1", the voltage on the input node is kept low (Vss), such as is marked "1" in Fig. 1. On the other hand, it is set high for writing a "0", and a small amount of charge, corresponding to the difference in surface potentials under the I gate and H cell remains and constitutes a "fat zero". To control the "fat zero" level, the barrier is formed under the I gate. The signal is sampled when the clock I returns to the low level (time T3), and stored in the H cell. During the interval T4-T5 the charge in the H cell is spread and divided again by the S gate when the clock S goes low. As a result, the charge level of the C cell at time T5 is corresponding to the area ratio of the H and C cells. This charge splitting input method makes it flexible to lay out the pattern of input stages. Therefore this concept is very useful to CCD memory.

Figure 2 is a photomicrograph of input stages for 4-channel multiplex. Alternate arrangement of the I gates advances packing density of channels. Figure 3 shows the pulse wave forms to operate these input stages. Figure 4 shows the analog output from the each four multiplexed channels. Storage area at the H and C cells, calculated signal charge and output voltage of each channels are listed in Table 1. It shows that multiplex operation of 4 channels is accomplished successfully without crosstalking.

The photomicrograph of the 64K-bit CCD memory designed by this multiplex technique is shown in Fig. 5.

The chip has transfer clock generators and is all TTL-compatible. This device was desiged with 5μm-rule and fabricated by an n-channel double poly-silicon process, and mounted in an 18-pin package.

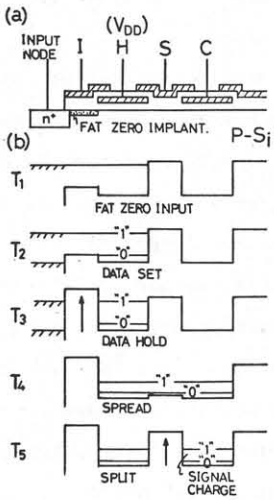

Table 1

	H cell (μm²)	C cell (μm²)	Calculated signal charge (pc)	Output voltage (v)
Ch. 1	84.5	82.0	0.16	1.2
Ch. 2	129	61.5	0.16	1.1
Ch. 3	129	61.5	0.16	1.1
Ch. 4	84.5	82.0	0.16	1.2

Fig. 1 The input stage
(a) cross section (b) surface potential

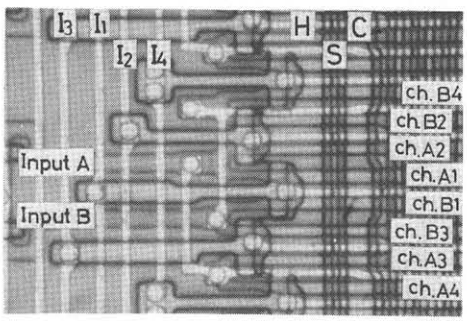

Fig. 2 Photomicrograph of the input stages

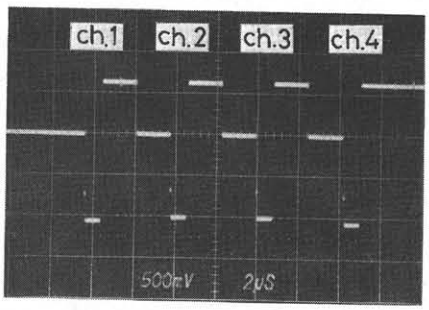

Fig. 4 Analog output from each channels

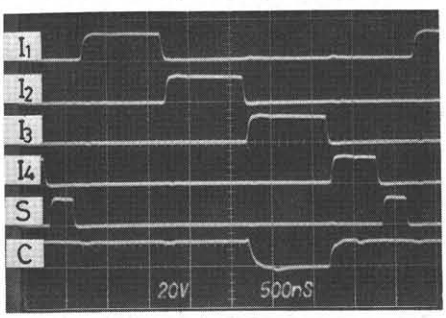

Fig. 3 Clock pulses generated on the memory chip for 4-channel multiplex

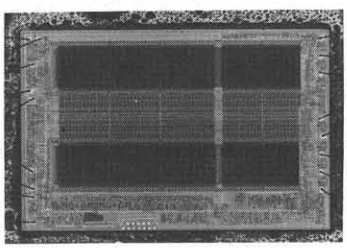

Fig. 5 Photomicrograph of the 64K-bit CCD memory