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# A — 6 — 3 CCD Analog-Analog Correlator with Four-FET Bridge Multipliers*

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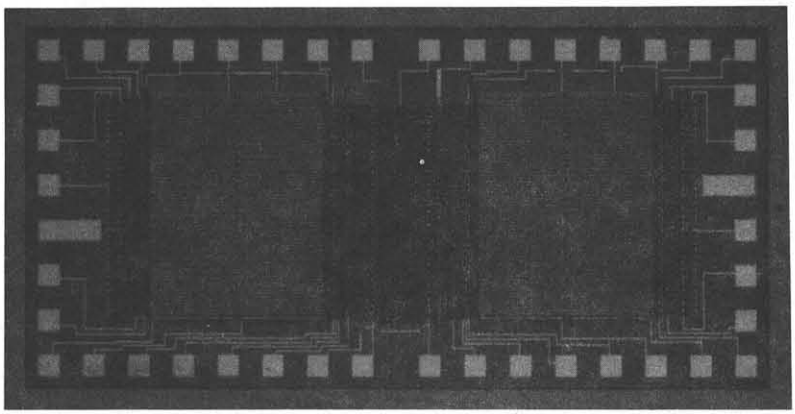
Design features and experimental results will be presented on a CCD-based monolithic analog-analog correlator using multipliers consisting of four MOSFET's in a bridge arrangement. A photomicrograph of a 32-stage prototype is shown below. The CCD's and multipliers are on a 30 μm pitch. Each analog input path consists of a dual-channel differential CCD with source-follower-buffered floating-gate non-destructive charge detectors. The principal advantages of this new approach are reduced sensitivity to the following sources of error in conventional designs: nonlinearities in the input stage and output taps of the CCD's and in the multiplier MOSFET's; shifts in CCD bias charge level; offsets due to dark current accumulation; fixed-pattern noise due to gradual spatial nonuniformities in dark current generation; and interstage variations in threshold voltages. The balanced multiplier configuration also allows smaller, lower power source followers to be used to buffer the floating gate outputs. Measurements on multiplier array subsections of the chip show distortion terms typically more than 50 dB below the product terms. Moreover, this high level of performance is maintained over a range of common-mode bias offsets up to several volts.



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