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REDUCED GEOMETRY GaAs CCD FOR HIGH SPEED SIGNAL PROCESSING

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Development of Charge Coupled Devices (CCD's) in III-V compounds, particularly GaAs, is advantageous since it opens up areas of application of high speed signal processing devices, as well as imaging devices, which are not easily accessible with silicon CCD's. GaAs based CCD's can be expected to have superior performance in high speed signal processing due to the higher electron mobility in GaAs. The higher mobility makes possible shorter (drift-aided) transit time for charges from under one gate to the next, thus increasing the maximum possible clock frequency. More importnatly, the higher electron mobility in GaAs makes high speed on-chip Fets for clock-drive and charge detection possible.

The difficulty in obtaining stable oxides in GaAs, however, has prevented development of a conventional M.I.S. (metal-insulator-semiconductor) CCD. The possibility of a buried channel Schottky-barrier gate CCD was suggested[1], and such a device has recently been realized[2,3] in GaAs. Moreover, this device has been shown to have high charge transfer efficiency[4]. This device differs from a conventional buried channel CCD in yet another significant aspect. Instead of the p-substrate, n-active layer arrangement typically used in buried channel CCD technology, this device employs a semi-insulating substrate and n-type active layer. The semi-insulating substrate has important implications for high speed applications since stray capacitance is reduced resulting in substantially lower power dissipation in the clock drivers ($P_d = c\ v^2\ f$). Also, the semi-insulating substrate eliminates the need for a separate channel stop.

The first device described in Refs. 2 and 4, was a 30 gate device and served as a demonstration vehicle designed to prove the concept of the Schottky-barrier gate, buried-channel CCD, and to characterize it with respect to transfer efficiency, linearity, and floating gate capability. A new device with 259 gates, shown in Fig. 1, has been fabricated and very recently operated. While detailed measurements are still in progress, the transfer efficiency has been verified to be >0.999 per transfer. This device employs 4.5μm x 100μm transfer gates (separated by 1μm gaps), as well as an on-chip reset amplifier. This amplifier is distinguishable in the right-hand extremity of the device. The CCD transfer gates are connected in a 4-phase configuration. The active layer of the device is n-type with $N_D = 1 \times 10^{16}/cm^3$. The device channel is isolated with a mesa etch and the electrode interconnection patterns are printed directly on the semi-insulating substrate. The device employs two-level metalization isolated by a plasma-deposited silicon-nitride.

Calculation of the minimum electric field, in the direction of charge transfer, under the gates correlated with measured electron mobility, indicates capability for charge transfer well in excess of 1 GHz without transit-time induced degradation in transfer efficiency. At present, preparations are under way to evaluate the performance of this device at high frequency (>100 MHz). The results of these experiments, as well as evaluation of linearity, charge capacity, and dark current uniformity, will be reported.

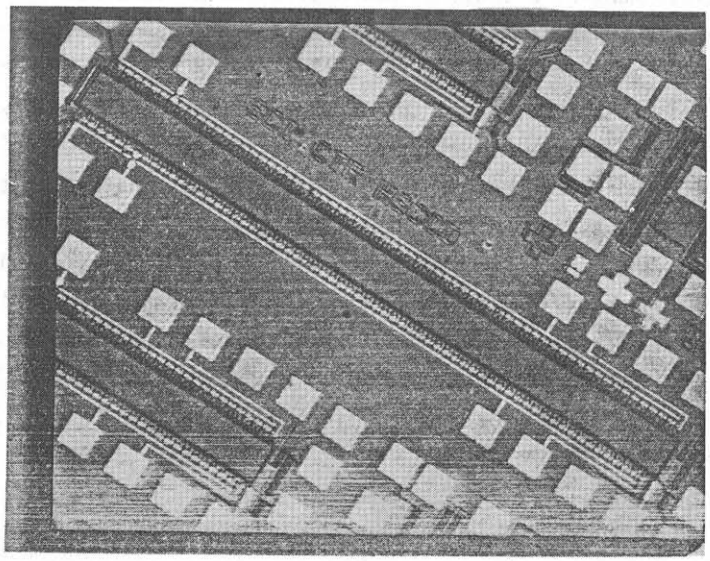

Fig. 1