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A — 6 — 5 Charge-Transfer Devices in HgCdTe/CdTe Heterostructure

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This paper reports on the demonstration of metal-insulator-semiconductor charge-transfer devices in epitaxial HgCdTe grown on CdTe substrates. The work focuses on the development of linear CCD shift registers in HgCdTe/CdTe heterostructures. CID devices are used to study the properties of the MIS structures in epitaxial HgCdTe.

Charge-transfer devices in epitaxial layers offer potential advantages over similar devices in bulk materials in the design of self-scanned imagers, especially for monolithic development. In bulk HgCdTe CCDs have been demonstrated earlier[1,2] for potential function as self-scanned infrared photocapacitors. However, these devices are limited to a frontside-illuminated configuration requiring transparent electrodes unless backside-thinned. The choice of CCDs in the HgCdTe/CdTe heterostructure facilitates the backside-illumination mode without the need for backside-thinning since CdTe has a larger bandgap than the epitaxial layer. The result is that high-density, mechanically-durable monolithic imagers can be designed which incorporate separate p-n junctions for optimum signal detection and on-chip CCDs for signal multiplexing. Backside-illuminated photovoltaic mosaics in HgCdTe/CdTe heterostructure for the long-wavelength (4-11 μm) region have been demonstrated.[3] In addition, CCDs in analogous epitaxial GaInSb/GaSb structures have been reported for 1.7 μm response.[4] HgCdTe has an important advantage over the III-V semiconductors such as GaInSb in that a wide range of alloy-composition-tuned energy gaps, to near zero, can be achieved with only a small variation in the lattice constant. The CID and CCD devices reported here are for $Hg_{0.7}Cd_{0.3}Te$/CdTe structures which have a 5 μm photoresponse cutoff at 77K.

The HgCdTe/CdTe structures used are n-type (undoped) $Hg_{0.7}Cd_{0.3}Te$ layers grown by liquid-phase epitaxy on (111)-oriented intrinsic CdTe substrates. The as-grown layers, typically 10 μm thick are smooth and inclusion free. Low carrier concentrations in the epilayer, typically 5×10^{14}-$10^{15} cm^{-3}$ (as determined from Hall and MIS C-V measurements) are achieved by low temperature annealing.

Charge injection devices are fabricated to study the electrical and optical properties of the MIS structures in HgCdTe epitaxial layers. The MIS CID devices consist of 2000 Å of ZnS evaporated onto surface-etched HgCdTe followed by

Cr-Au gate metallization. The corresponding flat-band voltages are very close to zero bias ($\lesssim 0.5$ volt) and estimated fast surface-state density is in the range of low $10^{11} cm^{-2} eV^{-1}$. The MIS structure is operated in the charge-injection mode by optically generating and storing minority carriers in the potential well and reading out the signal by injection of the stored charge into the substrate and detecting the resulting substrate current. From these measurements, charge storage times (a few seconds), dark current generation mechanisms, and spectral response are determined.

The CCD test structure is a 4-bit four-phase, 19-gate shift register with tunnel (or avalanche) breakdown input and floating gate output. The gates, (12 x 125 μm) are delineated within a channel stop boundary created by a Cr field plate. For the 4-phase device, the required double overlapping gate-insulator structure consists of first and second level ZnS insulator with thicknesses of 2000 Å and 4000 Å, respectively, with Cr gate metallization for both levels. Testing of the $Hg_{0.7}Cd_{0.3}Te$/CdTe CCDs is performed at 77K operating the device at a clock frequency of 25 kHz. Demonstration of charge transfer action is seen by the delay of the output signal relative to the input by the number of stages in the CCD. The charge transfer efficiency (CTE) calculated from the dispersion of the CCD output by summing the leading edge losses yielded a value of ~0.97. Interface trapping and transit time losses normally acoount for the transfer inefficiencies. However, for a hole mobility of ~ 200 cm^2/v-sec and a gate length of 12 μm, no transit time limitation on CTE is expected at a 25 kHz clock frequency. For the low interface state density of ~ $10^{11} cm^{-2} eV^{-1}$ a CTE > 0.99 is obtained from Lee and Heller's model[5] for the device structure. The observed CTE of ~0.97 is attributed to limitations in the test conditons.

CID and CCD charge transfer devices demonstrated in epitaxial $Hg_{0.7}Cd_{0.3}$ Te/CdTe heterostructures establish a new capability for realizing more versatile, self-scanned infrared imagers. In particular, the CCD capabilities shown in this work parallel the backside-illuminated photovoltaic mosaic development in HgCdTe/CdTe heterostructures. Together they demonstrate the feasibility of future monolithic intrinsic II-VI alloy imagers with on-chip signal processing. The CID and CCD device development in HgCdTe/CdTe heterostructures will be discussed in further detail.