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Static Induction Transistor Memory

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I. INTRODUCTION

Main conduction mechanism of static induction transistor (SIT) is a carrier injection control due to the potential barrier at the pinched-off intrinsic gate point, where the barrier height is capacitively controlled by the gate and the drain voltages in a basic operation [1]. One of the authors, J. Nishizawa, originately proposed the new dynamic RAM cell utilizing a vertically configurated SIT structure [2]. One of the source region and the drain region of SIT is set a floating region to realize dynamic RAM cell (SIT memory). Cell size of SIT memory is almost equal to that of single SIT, so that packing density becomes very high compared to the conventional memory such as double-level polysilicon dynamic RAM and VMOS dynamic RAM. Two operational modes of SIT memory are described here. One is the electron accumulation mode in which electrons are storaged in the floating cell region and another is the electron depletion mode in which electrons are removed from the floating cell region.

II. EXPERIMENTAL

We mainly measured the read-out speed, memory retention characteristics, and the temperature dependence of memory retention characteristics in two mode operations by using model device simulating single SIT memory cell. The model device comprises of 10 channels whose dimension is W × 200 μm (W = 5, 6, 7, 8, 9, 10 μm) at mask level. 36 bit dynamic SIT memory array whose input and output transistors are p-channel MOSFETs are also fabricated. Minimum cell size is 10 × 7 μm^2. In these model samples and cell-array samples MOS capacitor at the surface serves as storage capacitor. Read-out speed is measured by using the word line pulse having a rise time of 650 psec and displayed on a sampling oscilloscope having a rise time of 28 psec.

III. RESULTS

The retention time is observed over 10 sec in the electron depletion mode and is over 450 msec in the electron accumlation mode at room temperature as shown in Figs. 1 and 2. The retention time is reduced to 1.7 sec at 50° C and 300 msec at 75° C in electron depletion mode and is also reduced to 200 msec at 50° C and 30 msec at 75° C in electron accumulation mode. The more electrons are removed from the floating region, the larger reverse voltages are effectively raised between p^+ gate region and the floating region in electron depletion mode. On the other hand, the more electrons are accumulated in the floating region, the smaller reverse voltages are effectively biased between the p^+ gate region and the floating region in electron accumulation mode.

Read-out speed T_R in electron depletion mode is observed on an oscilloscope having a rise time of 0.8 nsec and illustrated in Fig. 3, where the read-out voltage ΔV_R and total read-out charge ΔQ are also plotted as a function of reverse gate bias voltages. This data is yet limited by the instruments. Read-out speed measurements are also made by using a sampling oscilloscope having a rise time of 28 psec. Read-out speed is about 600 psec ~ 800 psec in both operation. Read-out speed will be reduced by a factor of one due to the introduction of the modified impurity profile in the channel and the decrease of channel length. These basic performances hold in fabricated 6 × 6 bits memory array.

Dynamic random access memory action of fabricated 36 bit memory array is shown in Fig. 4, which shows that the read-out voltage difference for data "0" and "1" is about 320 mV at the output source follower node. In the SIT memory array, the bit line capacitor C_B can be made smaller than that of conventional memory such as double-level polysilicon d-RAM and VMOS d-RAM, so that cell sice can reduced and the number of cells per one bit line can be increased.

IV. CONCLUSION

The electron depletion mode is superior to the electron accumulation mode in the memory retention characteristics, its temperature dependency and operational tolerancy. Moreover, the bias voltage and the word line pulse amplitude in electron depletion mode is very small compared to those in the electron accumulation mode. Thus, SIT memory in the depletion mode is very promising in high speed VLSI. 16 Kbit and 64 Kbit d-RAM are now on market, where the double-level polysilicon structure is usually used. Basic operation in these memory cells corresponds to the electron accumulation mode descrived in this manuscript. Therefore, an introduction of the electron depletion mode even to the double-level polysilicon d-RAM can be estimated to improve its performances, i.e., increasing retention time, decreasing temperature dependence and lowering voltage level required for operation. SIT memory is very promising in VLSI due to high speed, high packing density, and high impedance, which is being measured to estimate the maximum scale for integration, especially due to extremely low power dissipation. MOS memory cell structure is also available which can also be applied for permanent memory systems.

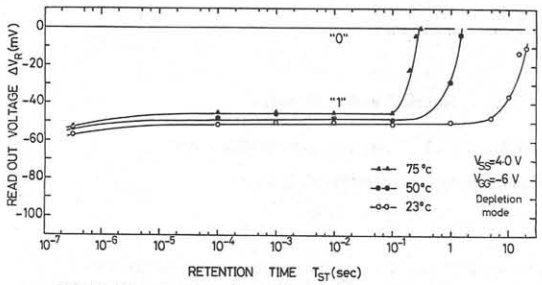

Fig. 1 Temperature dependence of memory retention characteristics in electron depletion mode. Read-out voltage ΔV_R, which is the difference of peak voltages between the two waveforms for data "0" and "1", is plotted as a function of retention time T_{ST} at write-in voltage V_{SS} = 4.0 V for three dirrerent temperatures of 23° C, 50° C and 75° C.

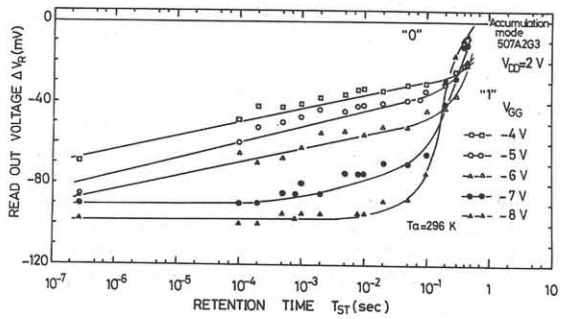

Fig. 2 Memory retention characteristics at 296 K in electron accumulation mode, read-out voltage ΔV_R versus retention time T_{ST} at write-in voltage V_{DD} = 2.0 V for five different reverse gate bias voltages.

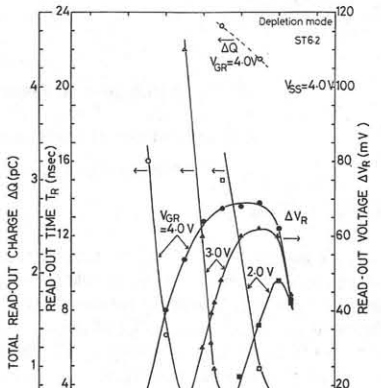

Fig. 3 Read-out time T_R, read-out voltage ΔV_R and total read-out charge ΔQ versus reverse gate bias voltage for three different word line pulse voltages of 2 V, 3 V and 4 V.

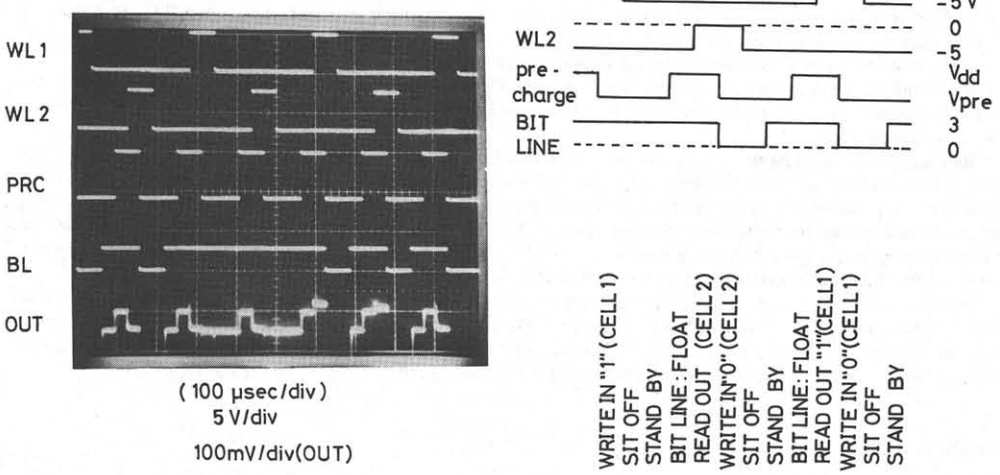

Fig. 4 Operational sequence and waveforms of 36 bit SIT memory array, read-out voltage difference for data "0" and "1" is about 320 mV.

REFERENCES

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