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Static Induction Transistor Logic

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I. INTRODUCTION The I^2L equivalent static induction transistor logic [1]-[4] (SITL) is evaluated by using type D F/F frequency divider and 14 bit BCD programmable counter to prove its potentiality in VLSI. Operational frequency is over 20 MHz in the frequency divider and 10 MHz in the 14 bit BCD programmable counter with a power dissipation of a few hundreds microwatts.

The normally-configurated SIT is introduced to serve as a driver transistor in the SITL having new circuit configuration in order to improve the speed performance, where output Schottky diodes are fabricated to ensure the decoupling among multi-outputs. The performance of this Schottky SITL is evaluated by using the inverter chain, where the propagation delay is 2.5 nsec with a power dissipation of 100 μW.

II. I^2L EQUIVALENT SITL The basic structure of the I^2L equivalent circuit has already been illustrated in the previous papers [1]-[3], which is characterized by very simple fabrication process. A type D flip-flop frequency divider with set and reset has been fabricated to evaluate the performance of the I^2L equivalent SITL. In the two stage frequency divider, the delay time is 45 nsec per stage and maximum input frequency is over 20 MHz. Figure 1 illustrates the relationship of input frequency to power dissipation of a six stage type D flip-flop frequency divider. It is seen from Fig. 1 that the dynamic range of power dissipation is very wide and nanowatt operation is possible with this sample. Power dissipation is 70 μW per gate at the input frequency of 10 MHz. Maximum input frequency is 17 MHz with a power dissipation of 250 μW/gate.

Capability of I^2L equivalent SITL has also been evaluated by 14 bit BCD programmable counter. Figure 2 shows its top view photograph and block diagram. The operational frequency is plotted as a function of power dissipation in Fig. 3. The maximum operational frequency is obtained about 12 MHz with a power dissipation of 340 μW.

III. SCHOTTKY SITL In the I^2L equivalent SITL, the inversely configurated BSIT (Bipolar mode SIT) [4] [5] is used as the driver transistor, where the substrate serves as the source region and the drain region is set at the surface. In BSIT as well as conventional SIT [6]-[8], the intrinsic gate giving rise to a potential barrier is desired as close to the source region as possible, in order to obtain excellent performances such as high current density, low drain voltage for the onset of current saturation, high current gain and small series resistance contributing to the negative feedback action [9]. Moreover, the impurity concentration in the source region must be as high as possible to increase the current density, because SIT is carrier injection device. Introduction of normally-configurated structure to BSIT easily satisfies these requirements. The source region is set at the surface in the normally-configurated structure. As for frequency characteristics and driving capability, the normally-configurated BSIT is usually superior to the inversely-configurated BSIT. Thus, the new integrated circuit configuration using the normally-configurated BSIT must be introduced to improve the performance of SITL.

Figure 4 illustrates the cross-sectional view (a) and the equivalent circuit (b) of the new SITL. It is seen from Fig. 4 that this samples have two outputs where Schottky diodes D_1 and D_2 are fabricated on the surface to ensure the decoupling between these two outputs. The burried n^+ region is the drain region of driver BSIT. The isolation region is p^+ region in this sample which is directly connected to the source region of BSIT by metal wiring. The impurity concentration and the dimension of the channel of BSIT are chosen to be completely pinched-off by the gate to channel built-in voltage, thus establishing a potential barrier. The emitter-base junction of lateral p^+np^+ bipolar transistor serves as a diode for the gate clamp. In this new integrated circuit, the resistor serves as a load. This circuit configuration is basically similar to ISL presented by Philips [10].

In order to increase the noise margin, the forward voltage drop of output Schottky diode is desired as small as possible. Aluminum is used as Schottky metal in this experiment. The forward voltage drop is about 0.4 V in the output Schottky diodes. The normally-configurated BSIT including output Schottky diode exhibits the saturating current voltage characteristic. The drain voltage for the onset of current saturation gradually increases with increasing the gate bias voltage in the forward direction. The saturation drain voltage becomes larger than 0.5 V for the gate bias voltages higher than a certain value. The saturation drain voltage is usually less than 0.1 V in the normally-configurated BSIT, so that the increase of the saturation drain voltage in the BSIT including Shottky diode comes from the property of output Schottky diode. This new integrated circuit is called Schottky SITL.

The Schottky SITL inverter chain having seven stages has been fabricated in order to evaluate the dynamic performance of Schottky SITL, where the fanouts are three. The propagation delay time is plotted as a function of power dissipation for this sample having three fanouts in Fig. 5. It is seen from Fig. 5 that the propagation delay is about 25 nsec for the power dissipations from 100 μW to 400 μW. In this Schottky SITL, the operation is almost fixed at the required condition, so that the dynamic range for operation is narrow. Representative propagation delay of ISL is 3.5 nsec at a current level of 400 μA [10].

These results indicate that the introduction of normally-configurated structure to driver BSIT improves the speed performance of SITL. The performance of Schottky SITL can be furthermore improved by decreasing the forward voltage drop of output Schottky diode and the series resistance between the burried drain region and the output Schottky metal. Decrease of cell size easily reduces the power dissipation.

IV. CONCLUSION The I^2L equivalent SITL has been evaluated by fabricating type D flip-flop frequency divider and 14 bit BCD programmable counter to demonstrate its capability in the field of VLSI.

Schottky SITL using the normally-configurated BSIT as a driver transistor is introduced to improve the speed performance of SITL. In the inverter chain evaluation, the Schottky SITL has exhibited the propagation delay of 2.5 nsec with a power dissipation of 100 μW. These performances are easily improved by introducing modified structure, where the forward voltage drop of output Schottky diode is decreased as small as possible, the emitter-base junction of lateral bipolar transistor is replaced by Schottky diode for the gate clamp and MOS FET serves as a load transistor.

In the same time, MOS SIT, which usually corresponds to the short channel pre-punch-through MOS FET, has very slight storage effect around the gate as has been expected in 1971 [11]. The storage capacitance is very small in MOS SIT, so that the operation speed can be estimated very fast in MOS SIT logic circuit.

REFERENCES [1] J. Nishizawa,Proc. 1976 Conf. Solid State Devices: Jap. J. Appl. Phys. Vol. Suppl. 16-1, pp. 158-162, 1977. [2] J. Nishizawa and B.M. Wilamowski, ibid. Vol. Suppl. 16-1, pp. 151-154, 1977, Tech. Dig. 1977 ISSCC. FAM 18.3, 1977. [3] J. Nishizawa, Proc. 1977 Conf. Solid State Devices: Jap. J. Appl. Phys. Vol. Suppl. 17-1, pp. 231-239, 1978. [4] J. Nishizawa, B.M. Wilamowski, M. Shimbo, Y. Mochida and T. Nonaka, to be published in IEEE J. Solid State Circuits. [5] J. Nishizawa, T. Ohmi, Y. Mochida, T. Matsuyama and S. Iida, Tech. Dig. of 1978 IEDM. pp. 676-679. [6] J. Nishizawa, T. Terasaki and J. Shibata, IEEE Trans. Electron Devices, Vol. ED-22, pp. 185-197, 1975. [7] J. Nishizawa and K. Yamamoto, ibid, Vol. ED-25, pp. 314-322, 1978. [8] Y. Mochida, J. Nishizawa, T. Ohmi and R.K. Gupta, ibid, Vol. ED-25, pp. 761-767, 1978. [9] J. Nishizawa, T. Ohmi, Y. Mochida and T. Matsuyama, to be published. [10] Electronics: pp. 41-42, June 8, 1978.

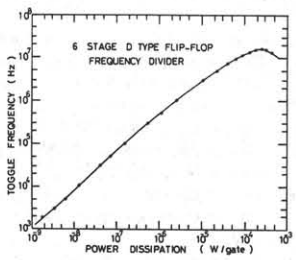

Fig. 1 Input frequency vs. power dissipations in the type D flip-flop frequency divider having six stages: Application of I^2L equivalent SITL.

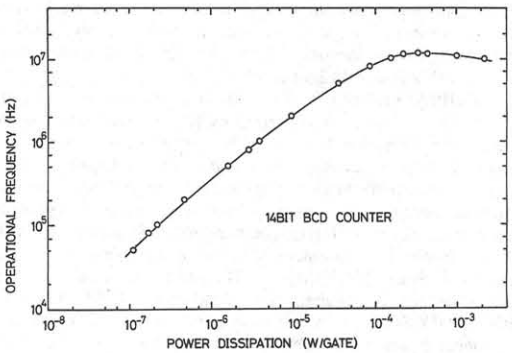

Fig. 3 Operational frequency vs. power dissipation in the 14 bit BCD programmable counter.

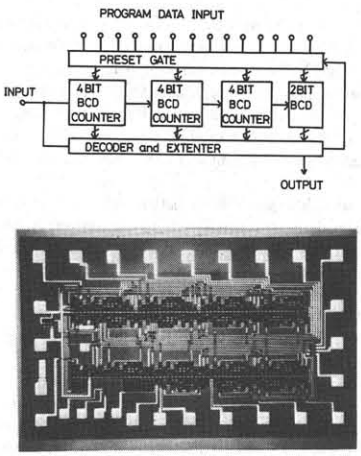

Fig. 2 Block diagram and top view photograph of 14 bit BCD programmable counter using the I^2L equivalent SITL.

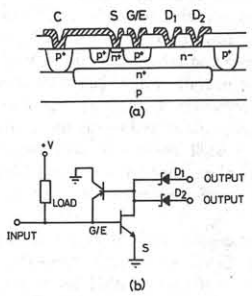

Fig. 4 Cross-sectional view and equivalent circuit of Schottky SITL.

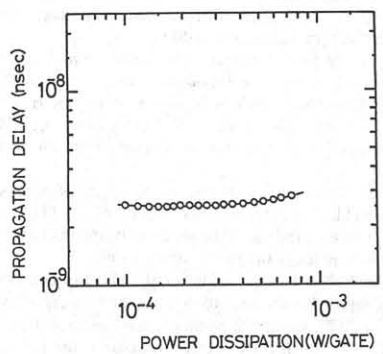

Fig. 5 Propagation delay vs. power dissipation of the Schottky SITL inverter chain.