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2 GHz, High Power Silicon SIT's

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1. Introduction

The SIT (Static Induction Transistor) was originally proposed by J. Nishizawa et al[1] in 1950, and recently has been proved to have capabilities as power devices above 1 GHz. We already reported on a Si SIT with a power output of 10 W at 1.2 GHz.[2] The output power has been, to the authors' knowledge, the highest power achieved so far with SIT's at and above 1.2 GHz.

This paper reports on a newly developed Si SIT with a power output of ∿10 W at 2.1 GHz, which has been realized by device fabrication improvements and circuit optimization.

2. Device Design and Fabrication Process

Fig. 1 shows the fundamental structure of developed SIT as a cross-sectional view. Gate (P^+) and source (N^+) regions were formed by preferentially diffusing B and As into an N/N^+ epitaxial wafer, respectively.

In order to make operating frequency higher, fine patterning techniques have been successfully used without lowering gate-to-source breakdown voltage V_{BSG}.

(1) Fine patterned structure (6.5μm pitch)

The "Washed Gate" process was employed to fabricate SIT's with 6.5μm pitch structure. Source and gate electrodes were formed by "Chemical Dry Etching" (CDE) of Mo and RF sputtering of Au to make a three layer structure of Au/Mo/Ti. Fig. 2 shows the source and gate electrodes. The width of source and gate electrodes are 2μm and 1.5μm, respectively.

(2) Improvement in structure between source and gate

The regions between source (N^+) and gate (P^+) regions were slightly etched and thermally oxidized to obtain higher transconductance (g_m), without lowering gate-to-source breakdown voltage V_{BSG}. Consequently, g_m was made to become about 1.4 times larger.

3. Experimental Results

Fig. 3 shows the current-voltage (I-V) characteristics of a 4 cell SIT. It exhibits intermediate I-V characteristics of triode and pentode,[3] which are suitable for high frequency high power operation. The electrical characteristics of 4 cell SIT are shown in table 1.

At higher frequency, SIT's have higher power gain with the gate grounded than with the source grounded. Fig. 4 shows the S-parameters of a grounded gate 1 cell

SIT. A maximum frequency of oscillation (fmax) was calculated to be about 6 GHz. As shown in Fig. 4, output impedance is relatively low. The 4 cell SIT we fabricated is internally matched at the output port to reduce power loss.

Fig. 5 shows the output power and drain efficiency of 4 cell SIT. Maximum output power is 9.1 W, with 3.6 dB gain and 30% drain efficiency at 2.1 GHz.

4. Reference

(1) Y. Watanabe, J. Nishizawa et al; Japanese Patent 205 068: published No.28-6077: Application Date Dec. 1950.

(2) K. Aoki, H. Kamo; Proc. Meeting of IECE, Japan (1976), P.2-55 (in Japanese).

(3) K. Aoki, H. Kamo; Proc. Meeting of the Japan Society of Applied Physics (Spring, 1976), 28a-N-7, P.368 (in Japanese).

V_{BSG}	20 V
V_{BDG}	60 V
I_D (V_{gs}= 0V, V_{ds}=10V)	1 A
g_m (V_{gs}=-2V, V_{ds}=10V)	200 ms
C_{gs} (V_{gs}=-5V)	13 PF
C_{dg} (V_{dg}=-40V)	9 PF

Table 1. Electrical characteristics of 4 cell SIT

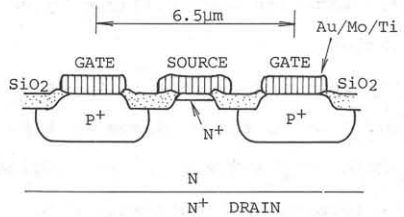

Fig. 1 Fundamental structure of SIT

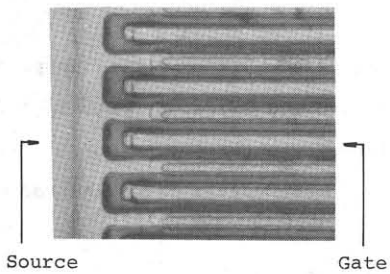

Fig. 2 Source and gate electrodes

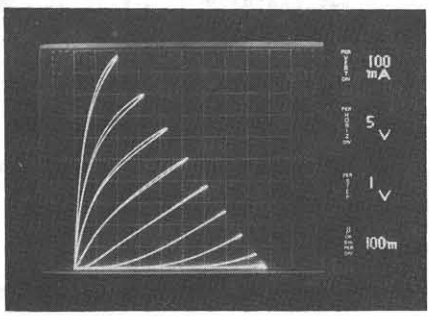

Fig. 3 I-V Characteristics of 4 cell SIT

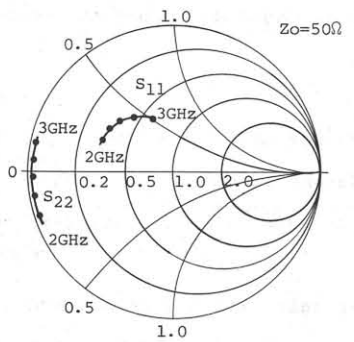

Fig. 4 S-parameters of 1 cell SIT

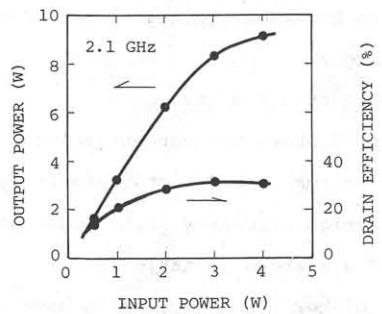

Fig. 5 Amplification characteristics of 4 cell SIT