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Bipolar Mode Static Induction Transistor (BSIT)

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I. INTRODUCTION Static induction transistor (SIT) has been confirmed experimentally and theoretically to be essentially excellent in high speed, high frequency and high power operations due to its fundamental characteristics [1]-[6].

Junction type SIT (JSIT) is easily designed as normally-off device, where the channel is completely pinched-off by the gate to channel built-in voltage, thus establishing a potential barrier in the channel. An application of forward gate bias voltage allows the drain current to flow. Normally-off JSIT is called bipolar mode SIT (BSIT). BSIT has been first applied to the I^2L equivalent static induction transistor logic circuit (SITL) [7]-[9], which is especially characterized by low energy operation.

BSIT exhibits the saturating current-voltage characteristic, while conventional SIT exhibits the non-saturating characteristic [7]-[10]. BSIT is characterized by high current gain, high transconductance, high current density and low drain voltage for the onset of current saturation [10]. Operational principle of BSIT is described here, especially concentrating on low impedance characteristic. BSIT is very promising to high current, high speed and high efficiency switching devices as well as low voltage and low energy integrated circuits.

II. BASIC OPERATION OF BSIT Brief design theory of BSIT using two-dimensional rectangular channel structure has already been described in the previous papers [9][11]. It is natural to require that the gate to gate spacing and the impurity concentration must be designed to realize the complete pinch-off of the channel due to the gate to channel built-in voltage. Moreover, the rate of the channel length to the gate to gate spacking is required larger than 0.7 in order to establish a potential barrier in the channel even when a certain drain voltage is applied. This rate must be increased to increase this blocking drain voltage [11].

Variations of JSIT from normally-on characteristic to normally-off have been confirmed experimentally by fabricating surface gate structure n-channel JSIT having six different gate to gate spacings. These samples have 10 channels comprizing of source length of 200 μm, gate diffusion depth of 2.6 μm, impurity concentration of 3.6×10^{13} cm^{-3} and epi-layer thickness of 4.7 μm. The gate mask spacing is changed by one micron step from 5 μm (ST4) to 10 μm (ST9). Figure 1 illustrates the relationship of drain current I_d to gate voltage V_g for these samples, where the drain voltage V_d is kept at 1 V. It is seen from Fig. 1 that samples of ST4 and ST5 are normally-off devices while samples of ST6 . . and ST9 are normally-on devices. Even in normally-on FSIT, the drain curretns start to increase rapidly with increasing forward gate bias voltages higher than about 0.5 V. In a high forward gate bias voltages, the drain current is not so strictly sensitive to the channel dimension in BSIT. There does not appear the rapid increase of drain current for high forward gate bias voltages in the conventional FET. SIT is an injection device where majority carriers are directly injected into the channel from the highly doped source region, thus accompanying a rapid increase of drain current for high forward gate bias voltages. Characteristic of this rapid increase enables the current density of BSIT to become comparable to or larger than that of bipolar transistor, although the impurity concentration of the channel is very low in BSIT.

BSIT exhibits the saturating current-voltage characteristics as shown in Fig.2, where the sample has 9900 channels comprizing of source length of 45 =m, gate diffusion depth of 2.2 μm, gate mask spacing of 5 μm, impurity concentration of 5×10^{13} cm^{-3} and epi-layer thickness of 12 μm. In the current saturation region, the drain current increases with the increase of gate bias voltage, almost following the equation $I_d \propto \exp(qV_g/KT)$. In the low drain voltages, the I-V characteristic of BSIT seems complicate. This complicate behavior stems from the minority carrier injection from the gate region to the channel. It is seen from Fig. 2 that the drain voltage for the onset of current saturation is less than 0.1 V for the gate bias voltages higher than 0.45 V and the drain current increases drastically by 7 or 8 orders of magnitude with an increase of drain voltages of 1 or 2 mV.

This drastic increase of drain current in BSIT can be explained by the negative feedback effect due to the vertual base resistance r_{V_b} existing between the gate and the channel, as shown in Fig. 3. Most of electrons injected from source region to channel flow into the gate region in the low drain voltages, forming a part of gate current. The gate current causes a voltage drop across the vertual base resistance, so that there remains high potential barrier at the center of the channel as illustrated by dashed line in Fig. 4 even if high gate bias voltage is applied in the forward direction. In this situation, if the drain voltage is increased over a certain value, injected electrons can cross over this potential barrier and flow into the drain. This decreases the gate current accompanying the decrease of the potential barrier, which enhances the increase of the amount of electrons crossing the potential barrier and flowing into the drain region. Thus, the negative feedback effect due to the vertual base resistance disappears accompanying the drastic increase of drain current.

III. SWITCHING PERFORMANCE The saturation drain voltage is very small in BSIT which has high transconductance. BSIT can be estimated, therefore, to exhibit high efficiency switching performance. BSIT having 790 channels has been fabricated and mounted in a high frequency package, where the channel structure is as follows ,source length of 30 μm, gate spacing at mask level of 6 μm, gate diffusion depth of 2.6 μm, impurity concentration of 2.7×10^{13} cm^{-3} and epi-layer thickness of 6.8 μm. Cell size is 800×520 μm^2.

Switching waveforms of drain voltage and gate voltage are shown in Fig. 5, where the sample having three cells are used, the load resistance is 1 Ω and switching occurs between twice states of (20 A, 0.6 V) and (0A, 21 V). T_{off} is 220 nsec and 50 nsec for $V_{gdc} = 0$ V and -5 V, respectively. The turn off time of 30 A is 110 nsec under the condition of $V_{gdc} = -6$ V. The forward voltage drop is about 0.8 V for the drain current of 30 A. It can be concluded from these results that BSIT exhibits high current, high speed and high efficiency switching performances.

IV. CONCLUSION Operational principle and characteristic of BSIT has been described concentrating on low impedance, low saturation drain voltage and high transconductance. BSIT has been demonstrated experimentally very promising to high current and high speed switching devices as well as low voltage integrated circuits.

REFERENCES [1] J. Nishizawa, Tech. Dig. of 1972 IEDM. [2] J. Nishizawa, T. Terasaki and J. Shibata, IEEE Trans. Electron Devices, Vol. ED-25, pp. 185-197, 1975. [3] J. Nishizawa and K. Yamamoto, ibid, Vol. ED-25, pp. 314-322, 1978. [4] Y. Mochida, J. Nishizawa, T. Ohmi and R.K. Gupta, ibid, Vol. ED-25, pp. 761-767, 1978. [5] Y. Kajiwara, K. Horikiri, Y. Yukimoto, G. Nakamura and M. Aiga, Proc. 1978 MTT Int. Microwave Sym. D5-7. [6] T. Ohmi, J. Nishizawa and M. Tatsuta, Tech. Dig. of 1978 IEDM Late News. [7] J. Nishizawa and B.M. Wilamowski, Proc. 1976 Conf. Solid State Devices, Jap. J. Appl. Phys., Vol. Suppl. 16-1, pp. 151-154, Tech. Dig. of 1977 ISSCC, pp. 222-223. [8] J. Nishizawa, Proc. 1977 Conf. Solid State Devices: Jap. J. Appl. Phys., Vol. Suppl. 17-1, pp. 231-239, 1978. [9] J. Nishizawa, B.M. Wilamowski, M. Shimbo, Y. Mochida and T. Nonaka, to be published in IEEE J. Solid State Circuits. [10] J. Nishizawa, T. Ohmi, Y. Mochida, T. Matsuyama and S. Iida, Tech. Dig. of 1978 IEDM, pp. 676-679. [11] T. Ohmi, RIEC Tech. Rep. TR-43, 1979.

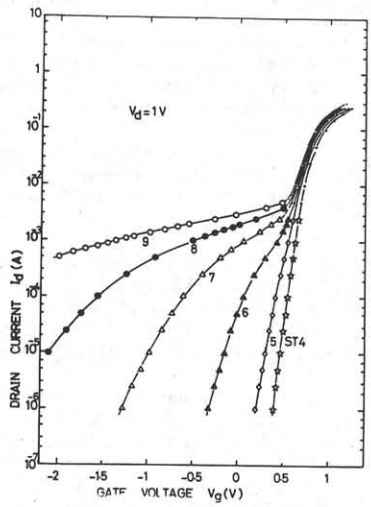

Fig. 1 Drain current vs. gate voltage of JSITs having six different gate spacing.

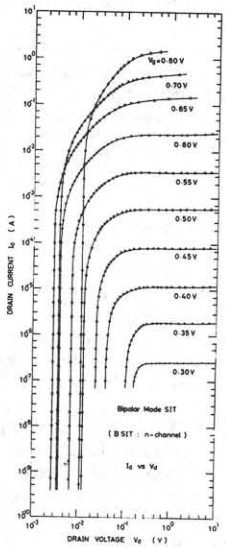

Fig. 2 Drain current vs. drain voltage of BSIT.

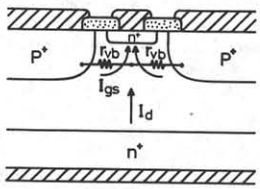

Fig. 3 Negative feedback effect due to the vertical base resistance r_{Vb}.

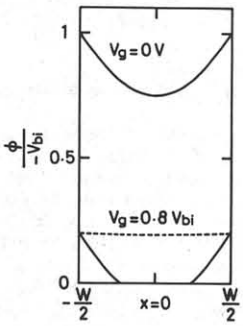

Fig. 4 Potential profile in the Cross-sectional direction of the channel. Dashed line: potential profile due to the negative feedback effect of r_{Vb}.

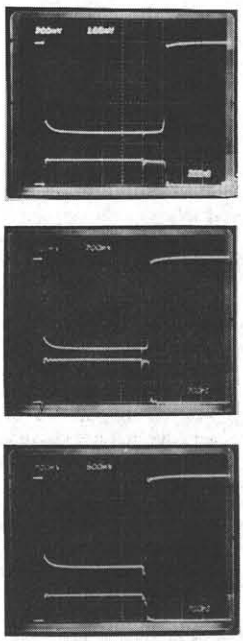

Fig. 5 Switching waveforms of drain voltage (upper trace: vertical scale 4.55 V/div) and gate voltage (lower trace). Horizontal scale: 200 nsec/div, T_{off} = 220 nsec, (b): V_{gdc} = -3 V, lower trace: 1.8 V/div, T_{off} = 90 nsec, (c) V_{gdc} = -5 V, lower trace: 4.5 V/div, T_{off} = 50 nsec.