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LSI Prospects for GaAs FET's*

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Semiconductor technology is striving to achieve performance at gigabit rates in logic operations. This goal requires microwave devices in monolithically integrated circuits. As the device dimensions become smaller for faster operation, the requirement for low power dissipation per device to prevent excessive heating of the chip becomes increasingly stringent when LSI is to be accomplished. The 1980's promise to be another era for semiconductors and especially integrated circuits with VLSI as the goal. The prospects for GaAs FET's are good to capture a position in this development and the success depends entirely on the availability of a high yield technology for large device density circuit fabrication.

With gigabit electronics¹ emerging as a branch of semiconductor technology, GaAs certainly is gaining momentum over Si when focusing on the prerequisites to satisfy the requirements for LSI. Low power and high speed small scale integrated (SSI) and medium scale integrated (MSI) circuits have been fabricated with depletion mode Schottky barrier FET's,^{2,3} with enhancement mode junction FET's,⁴ and enhancement mode Schottky barrier FET's.⁵ Developments are in progress which aim at the large scale integration (LSI) of GaAs FET's for gigabit logic applications not accessible with Si based device and integrated circuit technology.

A planar GaAs integrated circuit technology for 1 μ m channel geometries was realized for the enhancement mode JFET⁴ and the depletion mode MESFET⁶ by means of selective ion implantation of n- and p-type impurities into semi-insulating GaAs substrate materials. Figure 1 presents a scanning electron microscope picture of a portion of a planar GaAs positive edge triggered flip-flop fabricated with 2.5 and 1 μ m channel E-JFET's. The ion implantation process is the key to low threshold voltages for E-JFET's and low pinch-off voltages for D-MESFET's in order to achieve low power dissipation per gate and control of device uniformity over large wafer sizes. Photolithography imposes limits on fabrication yields, level of integration for the 1 μ m channel devices and small line width interconnections. Electron-beam lithography is in the offing of overcoming these constraints and will open new perspectives for LSI and eventually VLSI.

With optimized gate structures the gigabit logic capability of GaAs FET's was demonstrated with SSI and MSI circuits. LSI is, however, only achievable by reducing the power dissipation per gate to values in the range of 100 to 200 μ W. The logic family, exploring GaAs MSI and LSI, consists of the following members: BFL (= buffered FET logic),² SDFL (= Schottky diode FET logic)³ and DCFL (= direct coupled FET logic).^{4,5} Projections for the GaAs logic family are presented in Figure 2, which also contrasts the GaAs performance to the Si technology based integrated circuits. To qualify for gigabit LSI a propagation delay-power product of less than

100 femto-Joules is required, hence the delay-power product per gate is the important figure of merit for characterizing the logic gate performances. The dominance in speed of GaAs is obvious from Figure 2 and combined with low power dissipation yields a trade-off between Si and GaAs. With a choice of equal power dissipation, GaAs circuits possess a 4 to 5 times higher speed than Si ones and for equal switching speeds a vastly reduced power consumption for GaAs circuits is possible, thus establishing a basis for GaAs gigabit logic at LSI levels.

Considerable efforts are deemed necessary in logic gate optimization to obtain maximum speed at minimum power, exploration and refinement of processes, such as ion implantation, electron-beam lithography, high resistivity substrate material growth and perhaps molecular beam epitaxy, before GaAs technology reaches the maturity of Si technology now successfully applied to produce VLSI. Just as the planar technology has triggered the evolution of Si integration technology, now highlighted by VLSI, the planar GaAs technology has established the vanishing point of a perspective for GaAs integrated circuits with excellent prospects for gigabit LSI to unfold in the 1980's.

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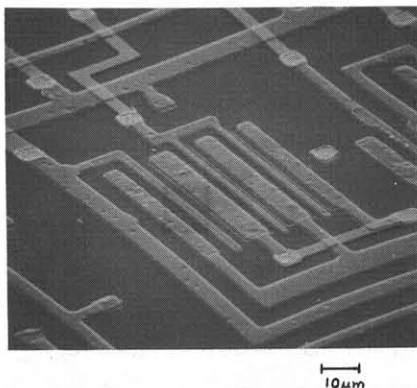


FIGURE 1 SEM Photograph of Planar IC Technology with 2.5 and 1.0 μ m Channel E-JFET's. (MAG x 1000)

