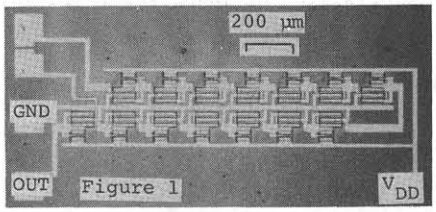
B—1—3 Low-Power High-Speed Integrated Logic with GaAs MOSFETs

Naoki Yokoyama, Takashi Mimura, Hirotsugu Kusakawa
Katsuhiko Suyama, and Masumi Fukuta

Fujitsu Limited
1015, Kamikodanaka, Nakahara-ku, Kawasaki 211 Japan

Recently, femto-joule pico-second integrated logic circuits have been pursued with normally-off-type GaAs MESFETs[1]. These circuits have a basic limitation in available logic voltage swing (~0.6 V) due to the onset of Schottky gate conduction. The use of a GaAs MOSFET technology avoids this limitation and allows more flexibilities in the circuit design. In this report, low-power high-speed integrated logic circuits with normally-off enhancement n-channel GaAs MOSFETs are demonstrated and a GaAs MOSFET logic is assured to be promising by comparing the speed/power performance of these circuits with other GaAs high-speed logic circuits.

Two types of GaAs MOSFET 13-stage ring oscillator, E/E type and E/D type, were fabricated using a low-temperature plasma oxidation technique[2] for gate insulation. The device geometries are shown in Table I with equivalent circuits of the unit inverter. Figure 1 is a photograph of the completed E/D type ring oscillator. Figure 2 presents transfer characteristics of the E/D type inverter with a DC supply voltage V_{DD} as a parameter, where the input is a triangular wave of 100 kHz. It is found that a transfer



A photograph of the E-D type 13-stage GaAs MOS ring oscillator.

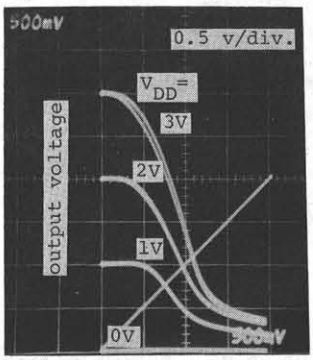


Figure 2 Transfer characteristics of the E-D type inverter.

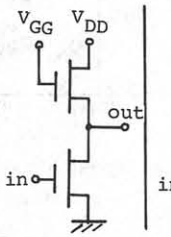
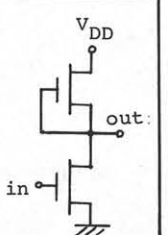
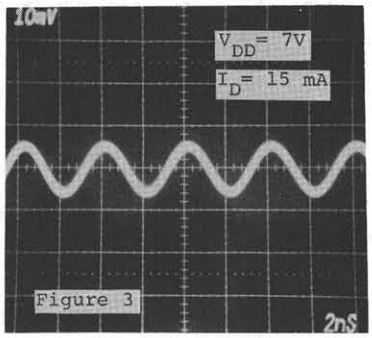
type	E/E	E/D
gate length	1.5 μm	2.0 μm
gate width driver	100 μm	200 μm
gate width load	10 μm	80 μm
equivalent circuit		

Table I Device geometries and equivalent circuits of the unit inverter.

gain and a logic voltage swing are proportionally increased with the supply voltage V_{DD}. When the supply voltage is 3 volts, the maximum transfer gain of 3 and the logic voltage swing of 2.7 volts are obtained.



Voltage waveform of the E-D ring oscillator.

Figure 3 shows a typical voltage waveform of the E-D ring oscillator at buffered output for the supply voltage V_{DD}= 7 volts. From the oscillation frequency and operating conditions, it is calculated that a delay time and a power-delay product are 150 ps and 1.1 pJ. The minimum delay time is 110 ps. From the E/E type ring oscillator, a delay time of 385ps and a power/delay product of 26fJ are obtained. Figure 4 shows a comparison of the speed/power performance of these circuits with other GaAs high-speed logic circuits. The filled circles show the performance obtained here. The shaded areas are projected status for 0.5 μm- and 0.2 μm- GaAs MOSFET logics assuming that the delay time is inversely proportional to the gate length. It is clear that the GaAs MOSFET logic is promising for low-power high-speed integrated logic circuits. Considering the flexibility in the circuit design, the GaAs MOSFET logic can be expected to become the most practicable one in the fields of a very high speed large scale integration when some problems of gate oxides for GaAs such as inability to reach strong accumulation and charge injection instability are solved.

This work was supported in part by the Ministry of International Trade and Industry of Japan.

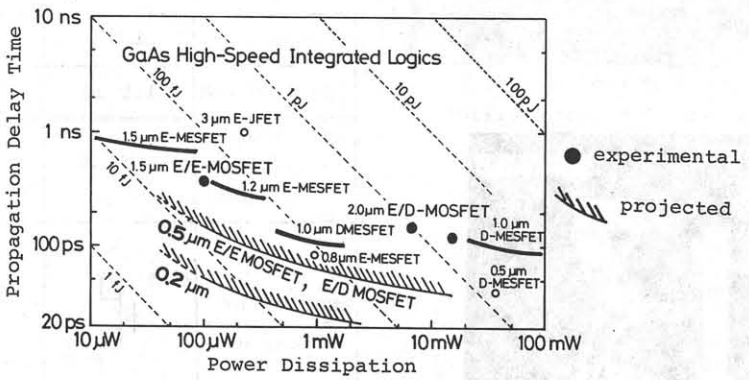


Figure 4 Speed/power performance of GaAs MOSFET logic with other GaAs high-speed integrated logic circuits.

(1) K. Suyama, H. Kusakawa, and M. Fukuta, Proceedings of the 10th Conference on Solid State Devices, Tokyo, 1978; Japanese Journal of Applied Physics, vol. 18 (1979) Supplement 18-1, 145-149.
(2) N. Yokoyama, T. Mimura, K. Odani, and M. Fukuta; Appl. Phys. Lett. 32(1) 1 January (1978) 58-60.