High-Speed Enhancement-Mode GaAs MESFET Integrated Circuits

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The performance of enhancement-mode GaAs MESFET logics will be described. A minimum propagation delay time as low as \( t_{pd} = 77 \) ps was obtained with power dissipation of \( P = 977 \) kW. The speed is the highest ever reported among the enhancement-mode GaAs FET logics. A liquid nitrogen temperature operation was also performed and the delay time of 51 ps was obtained.

Experiments

An epitaxially grown n-layer with carrier concentration of \( 1.2 \times 10^{17} \) cm\(^{-3} \) was mesa etched for electrical isolation. Ohmic contacts were AuGe-Ni alloys. Al and Ti-Au were utilized for Schottky-barriers and interconnects, respectively. The gate pattern was delineated by an electron beam direct writing. A projection mask aligner was employed for the other pattern delineation. The gate length was 0.8 \( \mu \)m and the gate width (\( W_g \)) was 20 \( \mu \)m or 40 \( \mu \)m. Figure 1 shows a microphotograph of a test inverter which consists of a 15-stage ring oscillator (RO), a monitoring FET and a 2-stage inverter for a transfer characteristic measurement.

Figure 2 shows a waveform of a 15-stage RO with \( W_g = 40 \) \( \mu \)m at supply voltage \( (V_{DD}) = 2 \) V. The propagation delay time is calculated from the period to be 77 ps at the power dissipation of 977 kW. Dependence of \( t_{pd} \) and power-delay product \( (P \cdot t_{pd}) \) on \( V_{DD} \) is shown in Fig. 3. The minimum \( P \cdot t_{pd} \) is 3.3 fJ (163 ps) at \( V_{DD} = 0.4 \) V.

For the reduction of \( P \cdot t_{pd} \), measurements were also made on a similar 15-stage ring oscillator with smaller \( W_g \) of 20 \( \mu \)m. The achieved minimum \( P \cdot t_{pd} \) was 1.6 fJ with \( t_{pd} = 200 \) ps. The minimum \( t_{pd} \) was 110 ps. The decrease in speed with decreasing the gate width was caused by parasitic capacitance and twice larger load resistance.

A liquid nitrogen temperature (77 K) operation on the \( W_g = 20 \) \( \mu \)m RO was performed to improve the \( t_{pd} \), taking advantage of high electron mobility. Twice higher speed than that at 300 K was attained. The minimum \( t_{pd} \) was 51 ps at \( V_{DD} = 3 \) V with \( P = 1.9 \) mW. The dissipation power also increased due to the current increase.

The above results are summarized in Fig. 4 as a \( t_{pd} \) versus \( P \) relation, comparing them with those of other reports. The results obtained here stand at the bottom left of the chart. The depletion mode GaAs MESFETs have shown the highest speed of 34 ps,\(^{(1)} \) but with nearly two orders of magnitude higher power.

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\(^{(1)} \)
dissipation than enhancement-mode FETs. The speed attained in this report is the highest among the enhancement-mode GaAs FET logics. By reduction of the gate length less than 0.5 μm, the tpd less than 50 ps will be possible.

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References (1) P. T. Greiling et al., Device Research Conf., 1978
(2) H. Ishikawa et al., ISSCC, 1977, p. 200

![Fig. 1](image1.png)

**Fig. 1** Microphotograph of a test circuit consisting of a 15-stage ring oscillator and a monitoring inverter

![Fig. 2](image2.png)

**Fig. 2** Output waveform of a ring oscillator

![Fig. 3](image3.png)

**Fig. 3** Propagation delay time and power-delay product as a function of a supply voltage

![Fig. 4](image4.png)

**Fig. 4** Propagation delay time versus power dissipation comparing the result presented here with those of other reports, solid line: Wg = 20 μm, broken line: Wg = 40 μm