B—1—7 Flip-Chip Mounted GaAs Power FET with Improved Performance in X to Ku Band

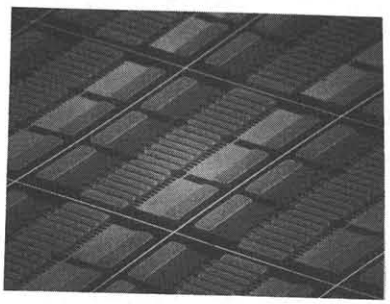
Y.Mitsui, M.Kobiki, M.Wataze, M.Otsubo, T.Ishii and S.Mitsui
Semiconductor Laboratory, Mitsubishi Electric Corporation
4-1, Mizuhara, Itami, Hyogo, 664 Japan

Introduction By progress in GaAs power FET technology, devices with a power output of 2.5 W at 8 GHz are now commercially available. However, devices with sufficient gain and power performances above X band are still difficult to achieve. A new type of GaAs power FET with extremely reduced parasitic inductances and good heat dissipation have been developed to realize improved r.f. performances in these frequency range. As a result, performances of 2.5 W at 15 GHz and 4.1 W at 12 GHz were obtained with the packaged devices.

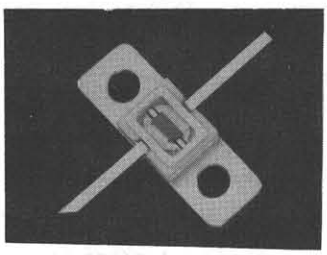
Device Structure Figure 1(a) shows a scanning-electron microphotograph of the chip with the metal posts plated on the source, drain and gate pads. Each unit cell has 1 μm gate length and 2400 μm gate width. The gate width is increased depending on the required power. The chip is turned over and all metal posts are connected directly to the corresponding bonding area in the package by thermo-compression bonding. Outside view of a 7200 μm gate FET (3-cells) mounted in a package is shown in Fig.1(b). As the source electrodes are soldered to Au-plated Cu heat sink, extremely reduced source inductances and good heat dissipation are realized, which lead to the improvement of the gain and power performances. Also, the simple assembly method gives high production yield.

FET Performance Figure 2 shows the typical input-output characteristics at 12 GHz and 15 GHz for 2- and 3-cells devices. The 2-cells device (4800 μm) operates even at 15 GHz with the linear power gain of 4.8 dB, a power output at 1 dB compression of 1.9 W and saturated power output of 2.5 W. A power output at 1 dB compression of 3.4 W is obtained at 12 GHz for 3-cells device (7200 μm). Figure 3 shows a frequency dependence of the linear power gain from 5 to 15 GHz for 1-cell and 3-cells devices. It is noted that the decrease in power gain is not remarkable up to 15 GHz by the new structure. Figure 4 shows the saturated power output and linear power gain at 10 GHz versus the total gate width. Decrease in power gain due to the increase in total gate width is not serious. The saturated power output increases linearly with the total gate width up to 9600 μm and saturated power output of 6.0 W is achieved at 10 GHz for 9600 μm gate device. The best results obtained are presented in Table 1.

Acknowledgement The authors wish to thank Dr.K.Shirahata for his encouragement through this work. We also gratefully acknowledge Mr.K.Segawa for supplying wafers and valuable discussions.



(a)



(b)

Fig. 1(a) Scanning-electron microphotograph of the FET chip.

Fig. 1(b) Outside view of a 7200 μm gate FET.

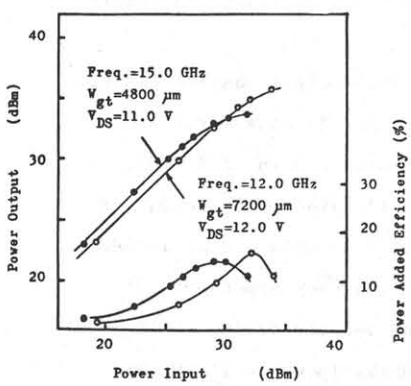


Fig. 2 Input-output characteristics at 12 GHz and 15 GHz for 2-and 3-cells devices.

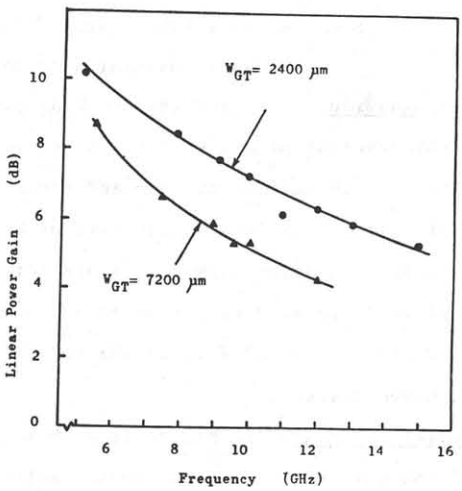


Fig. 3 Frequency dependence of the linear power gain.

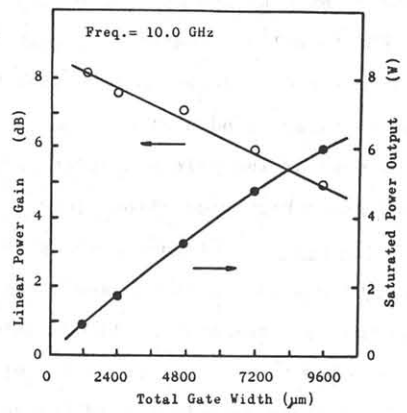


Fig. 4 Saturated power output and linear power gain at 10 GHz versus the total gate width.

Tab. 1 GaAs power FET performance.

Frequency f(GHz)	Power Output P_{1dB} (W)	P_{sat} (W)	Linear Power Gain G_{LP}(dB)	Power Added Efficiency η_{add}(%)	Total Gate Width W_{gt}(μm)
10	4.5	6.0	5.0	17	9600
12	3.4	4.1	4.0	16	7200
12	2.5	2.8	5.8	19	4800
13	1.2	1.5	6.0	17	2400
15	1.9	2.5	4.8	12	4800