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Interface Effects on Drain Current Instabilities in GaAs MESFETs with Buffer Layer

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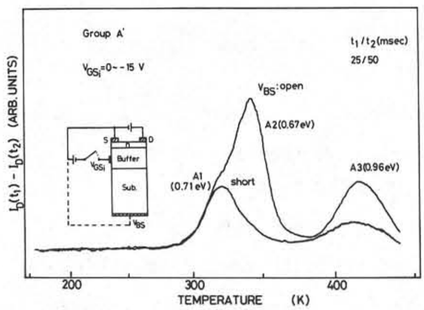
Anomalous phenomena such as substrate bias effect and long-term drift in drain current and RF parameters are frequently observed in many GaAs MESFETs. Recently it has been reported that hole traps in the vicinity of the interface between an active layer and a semi-insulating substrate can affect the channel resistance in GaAs MESFETs[1]. Insertion of a buffer layer is not always effective in eliminating the anomalies. We have previously reported the experimental investigations of the substrate bias effect on the drain current, its long-term drift characteristics and the correlations between them for three groups of GaAs MESFETs with a buffer layer[2]. It has been pointed out there that the long-term drift in the drain current (with the time constant of about 10 min at room temperature), which was ascribed to surface charges of the active n-layer, is rather due to the interfacial problems between an active layer and a buffer layer (A-B interface), between a buffer layer and a semi-insulating substrate (B-S interface), and the substrate with a buffer layer itself. In this report, the interface effects on the drain current instabilities have been further studied by applying Deep Level Transient Spectroscopy (DLTS) technique[3] to the drain current transients for the three groups of GaAs MESFETs (gated and ungated[2]).

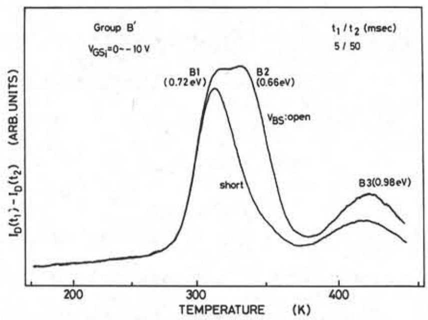
The DLTS measurements revealed that the drain current reduction or drift is caused by the formation of negative space charges due to hole emission from deep acceptors or hole traps, which exist at the both A-B and B-S interfaces, and also in the buffer layer and the semi-insulating substrate. Five kinds of deep levels were found for the three groups of FETs. Particularly it was clarified that the long-term drift in the drain current is attributed to the hole traps associated with chromium in the buffer layer as well as in the semi-insulating substrate.

In Fig.1(a),(b) and (c) are shown typical DLTS spectra of drain current transients due to gate-pad bias for the ungated FETs of each group. The disappearance of peaks A2 and B2 in the case of the substrate electrode short-circuited to the source may indicate that the corresponding traps are distributed near the B-S interface rather than the A-B interface, whereas A1 and B1 are located at the A-B interface side in the buffer layer.

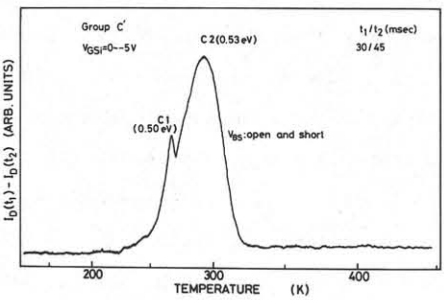
The long-term drift in the drain current was observed for Groups A' and B', but not for Group C'[2]. This is reflected to the fact that the peak corresponding to A3 and B3 was not observed for Group C'.



(a) ungated-FET,Group A'



(b) ungated-FET,Group B'



(c) ungated-FET,Group C'

Fig.1-DLTS spectra of drain current transients after the application of negative bias voltage to the gate-pad (electrode on the buffer layer).

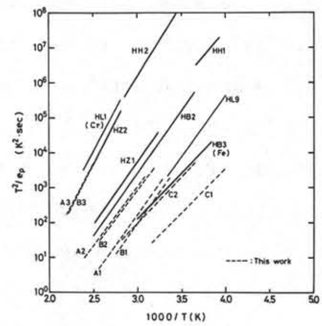


Fig.2-T^2/e_p against 1/T curves. HH1/HH2, data from ref.6); HL1/HL9, 4); HB2/HB3, 5); HZ1/HZ2, 1).

Comparison of the obtained emission rates with the published data of hole traps is shown in Fig.2. A3 and B3 are the deep acceptors attributed to Cr, and C2 to Fe. A1 and B1 may be related to HL9 by Mitonneau et al.[4], and A2 and B2 to HB2 (Trap B) by Lang and Logan[5].

For the gated FETs of each group, similar DLTS spectra were obtained when negative bias voltage was applied to the gate. This suggests that the interfaces pronouncedly affect the performance of GaAs MESFETs even with a buffer layer.

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