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Fabrication of DC-SQUIDs and their characteristics for digital applications

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Introduction

Interferometer type Josephson junctions are noted as potential elements for logic and memory circuits [1,2]. Especially, two junction interferometer, i.e. DC-SQUID, is promising for a memory cell which memorizes the flux quantum, as well as for a sum or a carry generator in a parallel full adder circuit proposed by Hasuo and Dazai [3].

When we design a logic or a memory circuit mentioned above, a threshold characteristic of the DC-SQUID plays the most important role. This paper presents a design theory of the DC-SQUID.

Design of DC-SQUID

The threshold characteristic, i.e., a control current I_H dependence of a critical current I_C, is illustrated schematicallly in Fig.1. Interference patterns (vortex modes) are included in the envelope of the threshold characteristics of the junction itself. In order to apply the DC-SQUIDs to digital circuits, following parameters (cf. Fig.1) should be controlled as expected.

1. I_{HD} : the difference of the control current between two neighboring vortex modes.
2. I_{HV} : the control current which gives the bottom of the vortex mode.
3. I_{HE} : the control current which gives a node of the envelope of threshold characteristic.

We have analytically investigated geometrical parameter dependences of these parameters by taking account of the image current of the control current. Then, we have fabricated tunnel junction type DC-SQUIDs with various geometries and dimentions in order to confirm the validity of the analytical results, which are listed as follows.

$$I_{HD} = W_{eff}\Phi_0/\mu_0(d_0\ell_J + d_1\ell) \quad (1)$$

$$I_{HV} = W_{eff}\Phi_0/2\mu_0(d_0\ell_J + d_1\ell) + W_{eff}I_0/W_C \quad (2)$$

$$I_{HE} = W_{eff}\Phi_0/\mu_0 d_0 \ell_J \quad (3)$$

where, W_{eff} is given by

$$W_{eff} = W_C \quad \text{(with ground plane)} \quad (4)$$

$$W_{eff} = W_C(W_H + W_B)/W_B \quad \text{(without ground plane)} \quad (5)$$

Other notations are as follows. Φ_0 :the flux quantum, μ_0:the permeability, I_0 :critical current for one junction, d_0 :=($d_{ox} + \lambda_{LB} + \lambda_{LC}$, d_{ox} :oxide thickness of the junction, $\lambda_{LB}.\lambda_{LC}$:London's penetration depths of the base and the counter electrodes), d_1 :=($d_{ins} + \lambda_{LB} + \lambda_{LC}$, d_{ins} : thickness of the insulator of the inductive bridge), ℓ_J :length of the junction, ℓ :distance between two junctions, W_H :width of the control line, $W_B.W_C$:widths of the base and the counter electrodes.

Figure 2 and 3 show example of the fabricated SQUID characteristics. As shown in these figures, the SQUID in Fig.2 (SQUID-A) has a symmetric structure and that in Fig.3 (SQUID-B) has an asymmetric structure. I_{HD}, I_{HV} and I_{HE} can be measured from these figures. They are 6.6, 16.0, 53 mA for SQUID-A and 3.6, 12.0, 54 mA for SQUID-B, respectively. These values obtained by eqs.(1)-(3) are 6.1, 15.7, 54 mA for SQUID-A and 3.5, 11.5, 54 mA for SQUID-B, respectively. It can be seen that eqs.(1)-(3) correctly describes the threshold characteristics of DC-SQUIDs. Referring these results, we have developed a numerical calculation method of the characteristic of DC-SQUID whose junctions are represented by distributed circuit models. An example of the calculated characteristic is shown in Fig.4 for the SQUID-B.

Digital applications

In order to apply DC-SQUIDs to the full adder circuit, following two conditions should be satisfied. 1. The overlap of two neighboring vortex modes should not exceed two fold. 2. Many interference patterns should be included in the envelope of the threshold characteristic of the junction itself. Typical example of the DC-SQUID characteristic for the full adder is shown in Fig.5.

When the DC-SQUID is used as a flux quantum memory cell, the constraint is that three vortex modes should overlap at no external current. The SQUID satisfying this condition has been fabricated , and its memory operation has been successfully achieved as shown in Fig.6.

References

[1] R.F.Broom et al, Digest of ISSCC'78, p.60

[2] M.Klein et al, Digest of ISSCC'78, p.62

[3] S.Hasuo and K.Dazai, IECE (Japan), ED78-112, 1979

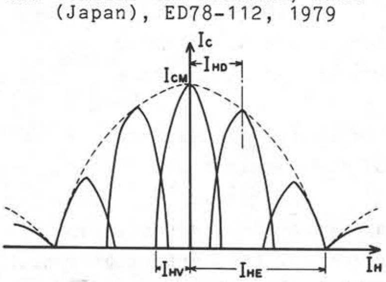


Fig.1 Schematic characteristic of a DC-SQUID

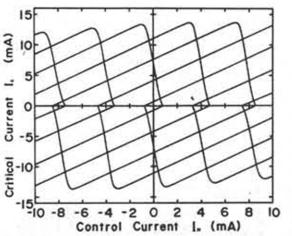


Fig.4 Calculated characteristic of a DC-SQUID of Fig.3

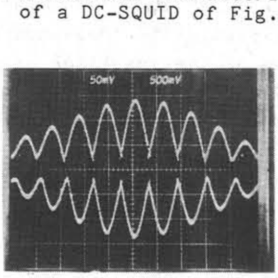


Fig.5 Threshold characteristic of a DC-SQUID for a full adder

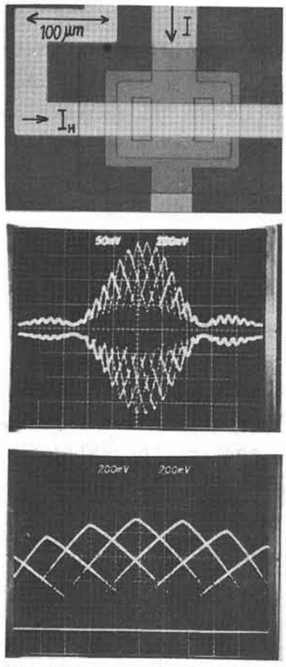


Fig.2 A symmetric SQUID characteristics. (V,H)=(5,20)mA/div (middle), (V,H)=(4,4)mA/div (lower, magnified)

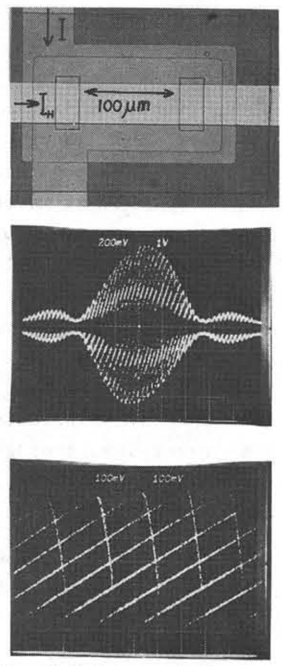
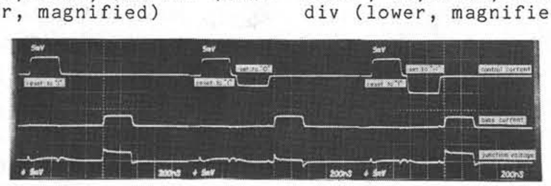


Fig.3 An asymmetric SQUID characteristics. (V,H)=(4,20)mA/div (middle), (V,H)=(2,2)mA/div (lower, magnified)



vert: 10mA/div (upper) 8mA/div (middle) 5mV/div (lower)

horiz: 200ns/div

Fig.6 Memory operation of a DC-SQUID. Upper, middle and lower traces show a control current, a bias current and a junction voltage waveform , respectively.